A Software Implemented Spread Spectrum Modem based on two TMS320C50 DSPs

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Abstract
A BPSK/DS-CDMA modem is described. Many functions of this spread spectrum modem are implemented in software on a DSP board. Constraints for proper IF receiver operation are given, plus BER measurement results for a prototype and a frequency-synthesizer resolution enhancement algorithm.

Brief description of the poster session
The poster session describes the design of a direct-sequence spread spectrum modem based on a signal processing board that contains a D/A-converter, an A/D-converter, and two digital signal processors (DSP) [2,3]. The spread spectrum signal is generated at baseband by multiplying each bit with the pseudo-noise code, so \( T_b = N_c T_c \) where \( N_c \) is the code length [chips]. The modulation scheme applied is BPSK with square-root raised-cosine pulse shaping of the chips (p1). The IF receiver demodulates the input signal at an intermediate frequency (e.g. \( f_{\text{IF}} = 128 \text{ kHz} \)) through coherent subsampling, using a software Costas loop for carrier tracking. This subsampling creates a baseband replica by spectrum folding (p2). The despreading also occurs in software by means of a serial search code acquisition scheme, and a delay-lock loop (DLL) for code tracking [6]. The proper operation of the DLL and Costas loop is determined by three constraints that concern the resolution of the sample frequency \( f_s \) and chip rate \( f_c \), the loop bandwidth \( B_L \) and the loop sample frequency \( f_s \) [1,4,5] (p3). A prototype version of the modem was built using one TMS320C25 DSP. This prototype can achieve 16 kchip/s and measurement results are presented of its bit error rate performance (p4). A new design of the modem uses two TMS320C50 DSPs. On this new modem a multiple correlator scheme can be implemented, in order to increase the sample frequencies of the loops, so \( f_s > f_s \) instead of \( f_s = f_s \). Furthermore, thanks to a smooth resolution enhancement algorithm, both the sampling frequency and the chip rate can be generated by means of the timers of the DSPs. The algorithm has a recursive structure and is implemented by means of a look-up table. The 0’s and 1’s in this table state whether the next timer period has to be \( T \) or \( T+1 \) \([\Delta T_{\text{min}}]\), and the size of the table determines the resolution enhancement factor (e.g. a factor 7). Together the two DSPs are expected to be sufficiently powerful to implement in software all functions of the baseband transmitter and IF receiver for chip rates up to 64 kchip/s (p5).

References
The BPSK / DS-CDMA transceiver

The baseband transmitter and modulator

- The IF receiver

Tasks:
- Demodulation
- Despreading
Demodulation by subsampling

- Digital I,Q downconversion, \( f_{fs} = \frac{4}{2m+1} f_{IF} \)

**Time domain:**

\[
T_n = \frac{T_{IF}}{4} \\
T_n = 3 \frac{T_{IF}}{4}
\]

\( \bullet \) = sample moment

**Frequency domain:**

Example

Baseband replica
Despreading by correlating with the code

**Functions:**
- 1 Code acquisition (coarse)
- 2a Code tracking delay-lock loop, DLL (fine)
- 2b IF carrier tracking Costas loop

**Constraints for the loops:**
- DLL: $\Delta T_{\text{min}} < \frac{1}{50N_d f_c}$, $\frac{\Delta T_{\text{min}}}{T_c} < 0.5B_L$, $B_L < \frac{f_s}{10}$
- Costas: $\Delta f_{\text{min}} < \frac{f_s}{50}$, $\Delta f_{\text{min}} < 0.5B_L$, $B_L < \frac{f_s}{10}$
Performance of the C25-transceiver

- BER measurement results:

- Chip rate: $f_c \leq 16$ kchip/s
  (due to limited processor capabilities)

- Bit rate: $f_b \geq 250$ bit/s
  (due to the minimum update frequency $f_s$ of the control loops)
  code length: $N_c = 63$ chips
The C50-transceiver

- Schematic diagram of the DSP board:

  ![Diagram](image)

- Expected performance:
  - $f_c = 64$ kchip/s
  - Increased $f_s$ by means of multiple correlators

- Particularities:
  - ADC samples switch
  - Two timers for generating $T_c$ and $T_{fs}$

  Resolution enhancement algorithm, e.g.:

  $0, 0, 0, 0, 0, 0, 0$
  $0, 0, 0, 0, 0, 0, 1$
  $0, 0, 1, 0, 0, 0, 1$
  $0, 1, 0, 1, 0, 0, 1$
  $0, 1, 0, 1, 0, 1, 0$
  $0, 1, 1, 0, 1, 0, 1$
  $0, 1, 1, 0, 1, 1, 1$
  $0, 1, 1, 1, 1, 1, 1$
  $0, 1, 1, 1, 1, 1, 1$