Timing error measurement for highly linear wideband Digital to Analog Converters

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Abstract—The switching characteristics of Digital to Analog Converter (DAC) unit elements can limit DAC dynamic performance at high speeds [1]. Unbalances and mismatches in clock, data and output networks create a non-identical environment for every current cell. Together with mismatch in current cell switching transistors and other non-idealities, this causes the switching characteristics of the current cells to be non-identical.

A new method for measuring the timing error is presented. The measurement method is shown to be insensitive to all important non-idealities in the DAC and the measurement circuit. Transistor level simulations show that the measurement accuracy is better than 125fs. Together with an ideal calibration loop, this measurement accuracy can lead to an average SFDR of more than 95dB when applied to an exemplary 12 bit 1GSps DAC.

I. INTRODUCTION

For high speed DACs, the dynamic performance, e.g. Spurious Free Dynamic Range (SFDR), degrades for high frequency input signals. One cause for this degradation is the non-identical switching behavior of the unit elements, according to [2]. Causes for non-identical switching behavior include: unbalances and mismatches in the clock distribution, data distribution and output networks, mismatch in the switching transistors and other non-idealities. An illustrative example is shown in Fig. 1. In this paper, the current steering DAC (CSDAC) is used as an example, because of its excellent high frequency behavior. However, the presented analysis and methods can easily be adapted for other DAC architectures.

Fig. 1. Various sources of timing errors in a typical current steering DAC

Fig. 2 shows the output SFDR versus input frequency relationship for different values of the timing error standard deviation. This figure is the result of a MATLAB simulation using an exemplary 12bit 1GSps segmented DAC with the 5 Most Significant Bits (MSBs) implemented using unary coding and the 7 Least Significant Bits (LSBs) with binary coding. The only non-ideal aspect of the DAC is the timing errors of the unary current cells. The saturation of the SFDR curves at lower input frequencies is due to the limited simulation accuracy. The dashed lines are extrapolations of the simulation results, showing the expected SFDR for lower input frequencies. These simulations clearly show the dependence of the SFDR on the value of the timing errors.

Fig. 2. Dependence of the average SFDR on the input signal for multiple values of the timing error standard deviation. A MATLAB model of a 12 bit, 5+7 segmented, 1GSps DAC with Gaussian distributed timing errors is used.

Some publications propose methods to reduce the effect of non-uniform switching behavior on the dynamic performance. The methods that are applied during the design phase (e.g. post layout mapping) cannot prevent the dynamic performance degradation due to process spreading. An exception to this rule is Dynamic Element Matching, which can counteract the effects of process spreading, but introduces extra noise [3].

On-chip integrated methods that measure the actual timing errors can potentially counteract all non-idealities. A phase detector is proposed in [4] to measure the glitch difference between a reference and the DAC current cells. However, it only measures the actual delay error, and does not take the non-identical transition waveforms into account. In [5], a measurement method is shown, which is based on analyzing the harmonics in the current cell response to a test signal. The analysis is done in the frequency domain.

In this paper, a new method for measuring the CSDAC timing errors in the time domain is presented. The next section discusses the proposed timing error correction loop. In section III, the proposed timing error measurement method is presented, which is a promising alternative to the published methods. An implementation of the proposed method is discussed in section IV along with simulation results.

II. ERROR CORRECTION LOOP

The timing error measurement method, presented in this paper, is part of a correction loop. A schematic overview of the correction loop is shown in Fig. 3, where the conventional DAC components are drawn in the hatched area. During normal operation, the current cells are connected to the output node, with output current I_{out} . When a current cell is being measured and calibrated, it is connected to the *Delay measurement* block. It can be shown that the mismatch between

Fig. 3. Timing error correction loop with DAC core hardware (hatched) and added timing measurement hardware

the normal switch cascode and the measurement cascode has a negligible influence on the timing error measurement.

The *Delay measurement* block measures the timing error between the connected DAC current cell and a reference current cell. A control loop adjusts the delay of the Variable Delay Latch (VDL) until the timing error between the two current cells is zero. An exemplary design of the VDL driver can be found in Fig. 4 [4]. In the following discussions, it is assumed that the effects of the finite calibration loop gain and the non-idealities of the VDL are negligible.

Fig. 4. Exemplary implementation of a VDL using digital control [4]

Since the reference current cell has a fixed output amplitude, only unary current cells can be calibrated. In the case of a segmented DAC with a certain minimum segmentation, it can be shown that the timing errors of the binary current cells have a negligible impact on the total dynamic performance [2]. Alternatively, in [4], it is suggested to calibrate the timing of all binary current cells plus one dummy LSB with one VDL.

The application of a control loop relaxes the requirements of the timing error measurement circuit. Instead of requiring a well defined gain and high linearity, strictly speaking only monotonicity is required.

III. PROPOSED EQUIVALENT TIMING ERROR MEASUREMENT METHOD

In this section, the timing error modeling and the timing error measurement method are discussed. Also the calibration of the measurement circuit is discussed.

A. Timing error modeling

An example of the transition waveform of a switching DAC current cell is depicted in the left waveform of Fig. 5. The transition waveform I_{tran} can be decomposed into an ideal

Fig. 5. The transition of a current cell and its modeled decomposition

step function I_{step} and a glitch I_{glitch} . The timing of the ideal step function is chosen such that the integral of I_{glitch} over time is zero. The delay of the ideal step function is introduced here as the 'equivalent delay' (d_{eq}). The difference between the equivalent delays of two current cells is defined as the 'equivalent timing error'.

The shape of I_{glitch} is not important [6]. Instead, the value of d_{eq} is of main importance to the output spectrum inside the band of interest. Therefore, current cell transitions will be characterized by their equivalent timing error.

B. Measurement method

The proposed equivalent timing error measurement method is based on the measurement of the charge difference between the transition of a reference current cell and the transition of the DAC current cell under measurement. It is implemented by integrating the difference between the output currents of these two current cells during a transition. To achieve insensitivity to amplitude mismatch between the two current cells, the current is integrated with switching polarity (see Fig. 6). The mathematical representation of the integration is given in (1), where V_{OS} is the offset voltage of the measurement circuit (e.g. the offset of the OTA in Fig. 8), I_{DAC} and I_{REF} are the output currents of the DAC current cell and the reference current cell respectively and V_{POL} is the integration polarity waveform.

$$V_M = V_{OS} + c \cdot \int_{-\infty}^{\infty} V_{POL} \cdot (I_{DAC} - I_{REF}) \cdot dt \quad (1)$$

The influence of the offset voltage in this integration is common to all current cells, hence it is omitted in the following calculations. To explain the switching polarity integration, a simplified picture of the two current cell waveforms and the polarity waveform is shown in Fig. 6. The difference between I_{DAC} and I_{REF} is shown as the dotted curve. During the high

Fig. 6. Simplified current cell waveforms and integration polarity

period of V_{POL} (from $-T_s + \epsilon_{t2}$ to $T_s + \epsilon_{t3}$), the equivalent timing error between the two current cells is integrated, but also the amplitude difference between the two current cells is integrated. During the two negative parts of the polarity waveform, the same amplitude difference is integrated with a negative polarity. The total sum of the integration will ideally be insensitive to the current cell amplitude mismatch.

The timing of the DAC current cell will be altered until the result of the integration is zero. The integration result can be rewritten to (2), where d_e is the timing error after calibration. The definition of d_R and d_D can be found in Fig. 6, A is the nominal output current of the current cells and c is the integration gain.

$$V_M = c \cdot (d_R - d_D + d_e) \cdot 2A \quad (2)$$

Ideally, the delay of the reference current cell d_R and the delay of the DAC current cell d_D are equal, and the calibration error d_e is zero. But due to non-idealities (for instance: current cell amplitude errors, offset and gain errors in the circuits, process mismatches and timing errors) the calibration error is not exactly zero. To simplify the expression for d_e , the definitions of (3), (4) and (5) are applied. The definition of α , β and ε_{tn} can be found in Fig. 6.

$$\left| \frac{\alpha - \beta}{\alpha} \right| = \delta P \quad (3)$$

$$\varepsilon_{tn} = \varepsilon_{tnb} + \Delta\varepsilon_t \quad \text{for } n \in \{1, 2, 3, 4\} \quad (4)$$

$$(1 - \delta P)(\varepsilon_{t4b} + \varepsilon_{t1b}) - (2 - \delta P)(\varepsilon_{t3b} + \varepsilon_{t2b}) = 0 \quad (5)$$

In (3), δP represents the relative amplitude error of the polarity waveform. (4) indicates that the timing errors of the polarity waveform are assumed to have a large common timing error ($\Delta\varepsilon_t$) and mutual timing differences (ε_{tnb}). (5) defines the value of $\Delta\varepsilon_t$ such that the equation for d_e is simplified. With all given definitions, the calibration error is expressed in (6). The definition of A , dA_N and dA_P can be found in Fig. 6.

$$\begin{aligned} d_e \approx & \frac{1}{2A} \cdot \{ \delta P \cdot T_S (dA_N - dA_P) \\ & + (d_R - \Delta\varepsilon_t)(dA_N + dA_P) \\ & + (dA_N - dA_P)((1 - \delta P)\varepsilon_{t1b} - (2 - \delta P)\varepsilon_{t2b}) \} \end{aligned} \quad (6)$$

The largest contribution to the calibration error is in the second line of (6), which consists of the amplitude error ($\frac{dA_N + dA_P}{2A}$) multiplied by the timing error between the reference current cell and the polarity waveform ($d_R - \Delta\varepsilon_t$). Based on the exemplary 12 bit 1GSps DAC and assuming a worst case amplitude error of 2% and $d_R - \Delta\varepsilon_t = 100\text{ps}$, the worst case average SFDR is approximately 70dB (see Fig. 2).

C. Polarity waveform calibration

A solution to the large calibration error of the previous subsection is to measure and calibrate the common timing error of the polarity waveform ($d_R - \Delta\varepsilon_t$). The polarity waveform calibration can be done in the same way as the calibration of the current cells. For this measurement, only the reference current cell waveform is integrated (see (1), with $I_{DAC} = 0$). When first applying the timing calibration of the polarity waveform and then the normal current cell calibration, the resulting calibration error is given in (7).

$$\begin{aligned} d_e \approx & -\frac{V_{OS}}{c\alpha 2A} \cdot \frac{dA_N + dA_P}{2A} + \left\{ \frac{dA_N - dA_P}{2A} \right\} \\ & \cdot \{ \delta P \cdot T_S + (\varepsilon_{t1b} - 2\varepsilon_{t2b}) \} \end{aligned} \quad (7)$$

The main contribution to the calibration error is the duty cycle errors in the polarity waveform ($\varepsilon_{t1b} - 2\varepsilon_{t2b}$) multiplied by the difference between the positive and negative amplitude errors ($\frac{dA_N - dA_P}{2A}$). Assuming the duty cycle errors are less than 20ps and the worst case $\frac{dA_N - dA_P}{2A}$ is less than 0.1%, the absolute value of the worst case calibration error is approximately 60fs. Extrapolation of Fig. 2 shows that this leads to an average SFDR of more than 100dB for the exemplary DAC. In practice, other phenomena will limit the SFDR to a lower value, but the SFDR is no longer limited by the timing errors of the DAC.

IV. CIRCUIT IMPLEMENTATION

This section discusses the circuit implementation of the equivalent delay measurement method.

A. Switched capacitor circuit

The method presented in the previous section is implemented for both the positive and negative current cell output transitions. The corresponding waveforms are schematically shown in Fig. 7. In this picture, the input current waveform

Fig. 7. Waveforms for measurement of positive and negative edge timing errors

$I_{measure}$ is the difference between the two current cell waveforms ($I_{DAC} - I_{REF}$) and shows an amplitude mismatch and a timing mismatch. $I_{measure}$ is integrated after multiplication with the polarity waveforms shown in the same picture; $V_{POL,PE}$ and $V_{POL,NE}$ are used to measure the positive and negative transition timing error respectively.

To reduce the number of control signals for the circuit, the polarity waveforms in Fig. 7 are different from the polarity waveform proposed in the previous section. In the negative phases, the integration gain is only half of the integration gain in positive phases, but the integration time is doubled. Hence, the result of the integration is identical to the polarity waveform of the previous section.

When using the switched capacitor integrate and dump technique, accurate polarity waveform implementation is possible. Fig. 8 shows a switched capacitor circuit which implements the equivalent timing error measurement method. To clarify the picture, only one branch of the differential circuit is shown. Also the initial condition reset switches are not shown.

This switched capacitor circuit is inside the *Delay measurement* block of Fig. 3. The input current $I_{measure}$, at the left side of Fig. 8, originates from the current cells. Since the input node can be connected to all current cells, a large parasitic capacitor C_{pd} is present.

The choices for the sizes of C_1 , C_2 , C_3 and C_{fb} are closely related, and together with the amplifier characteristics

Fig. 8. Circuit of the proposed timing error to voltage converter, only one branch of the differential circuit is shown

determine the accuracy of the discrete time integrator. This relationship is analyzed in [7], and leads to the following capacitor sizes: $C_{fb}=700\text{fF}$ and the other capacitors are 170fF .

First, the ideal operation without C_{pd} is explained, when only C_1 , C_2 and C_3 are used. The functionality of the other capacitors with the ‘a’ additive is explained later.

B. Normal operation

The switched capacitor circuit has an integrate and dump functionality. Capacitors C_1 , C_2 and C_3 integrate the input current in a particular phase. The integrated charge is dumped on the discrete time integrator, which is an Operational Transconductance Amplifier (OTA) with feedback capacitors C_{fb} . The discrete time integrator adds the integration results of different phases together.

C_1 integrates the input current during the positive part of both polarity waveforms, which is during ϕ_1 and ϕ_3 . During ϕ_2 , the charge of C_1 is dumped on the discrete time integrator for the positive edge (with output V_{op}) and during ϕ_4 on the negative edge integrator (with output V_{on}).

C_2 and C_3 are connected to the input during phases ϕ_2 and ϕ_4 . During ϕ_1 and ϕ_3 , C_2 is connected negatively to the positive edge integrator, implementing the negative part of $V_{POL,PE}$. In the same way, C_3 is used to implement the negative part of $V_{POL,NE}$.

After one cycle, the output of the positive edge integrator V_{op} is proportional to the charge difference between the positive edge of the DAC current cell under measurement and the positive edge of the reference current cell. The same holds for the negative edge integrator output V_{on} with respect to the negative edges of both current cells. The integration steps are repeated, accumulating the charge at the output of the discrete time integrators, and thereby increasing the signal to noise ratio.

C. Extended circuit

A problem with the switched capacitor circuit is the parasitic capacitance (C_{pd} in Fig. 8) at the input node of the switched capacitor circuit. This parasitic capacitance is charged to the same non-zero voltage as the integration capacitors. When a

transition between two phases occurs, the error charge left at C_{pd} is redistributed among the newly connected capacitors, introducing a non-zero initial error charge at the integration capacitors. Capacitors C_{1a} , C_{2a} and C_{3a} are added to measure and compensate the initial error charge. During a short interval at the beginning of every phase, an ‘a’ rated capacitor is connected to the input together with an integration capacitor, collecting an identical initial error charge. During the dump phase, the charge at the ‘a’ capacitor is used to compensate the initial error charge of the corresponding integration capacitor.

D. Simulation results

The presented equivalent timing error measurement method was simulated at transistor level using the exemplary 12bit 1GSps. These simulations confirm the calculated dependencies on the different non-idealities discussed in section III. However, due to the large dynamic range of the signals during the reference waveform calibration (see section III-C), the timing error measurement circuit shows non-idealities which are not taken into account in the calculations. Therefore, the calibration of the polarity waveform to the reference current cell is less accurate than calculated. Due to this non-ideal reference waveform calibration, the non-idealities mentioned in section III result in a worst case calibration error of 125fs, which is more than the expected 60fs. For the exemplary DAC, extrapolation of Fig. 2 shows that a timing error standard deviation of 125fs results in an average SFDR of more than 95dB.

V. CONCLUSION

A method for measuring the ‘equivalent timing error’ is presented. This method is shown to be insensitive to all common non-idealities of the DAC and the circuits. For a current steering DAC, an implementation using switched capacitor circuits is given. Transistor level simulations show a performance close to the expected value. The measurement accuracy of 125fs leads to an average SFDR of more than 95dB for an exemplary 12bit 1GSps DAC.

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