Lossless Multistage SOA Switch Fabric using High Capacity Monolithic 4x4 SOA Circuits

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Abstract: The first high data-capacity routing in a 3-stage switch using integrated 4×4 QW-SOA circuits is reported. The feasibility of a proof-of-principle 16×16 routing switch is demonstrated for 8λ×10Gb/s operation, with an IPDR of 6dB.

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OCIS codes: (130.4815) Optical switching devices; (250.6715) Switching

1. Introduction

In recent years, the increasing demand for multimedia communications has fuelled the need for greater network bandwidth. Although the growing use of photonics as a switching technology has been encouraging, commercial optical implementations have been restricted to slow speed devices such as MEMs based switches, which are also often lossy [1]. Alternatively, semiconductor optical amplifier (SOA) based photonic switches have attracted much interest owing to their ability to achieve lossless switching of high capacity data with nanosecond switching timescales. The use of SOA switches in WDM interconnects have been demonstrated using either discrete SOAs or integrated cross-point devices [2]. Most recently, several integrated 4×4 SOA switches have been demonstrated [3], though these have not to date allowed lossless operation suitable for WDM applications. In this paper therefore, we not only demonstrate a compact, lossless, integrated non-blocking 4×4 AlGaInAs QW SOA based crosspoint switch, but also investigate the feasibility of implementing 16×16 port count optical switches by cascading the 4×4 crosspoint switching elements.

2. Device details and static characterization

The crosspoint switch developed for this work has an active region which incorporates a 5 QW AlGaInAs structure which is grown on an InP substrate using MBE. The SOA gate structures in the crosspoint are ridge waveguides and they are interconnected with beamsplitters formed with tapered waveguides and deep etched mirrors to form a broadcast-and-select non-blocking tree architecture as shown in Figure 1. Each of the four input and output ridge waveguides has a width of 2μm. To realise the splitters, combiners and 90° bends, integrated beamsplitters and mirrors are formed using self-aligned ICP deep etching. The input and output SOA waveguides are each biased in common, to provide gain blocks to overcome coupling, splitting and waveguide losses, while the middle gating SOAs are each biased individually. The lengths of the paths through the switch vary from 1.55mm (path 1-1&4-4) to 2.8mm (path 1-4&4-1). The chip has an extremely compact footprint of 2.04mm×1.54mm.

Fig. 1. Photograph of the 4×4 switch. The tapered waveguides, beam splitter and internal turning mirror are shown as an inset

Continuous wave measurements have been carried out to investigate the DC characteristics of the switch. Up to 10dB fibre-to-fibre gain at 1550nm and a 3dB gain bandwidth of around 30nm are observed. [4]

3. Dynamic operation

To allow fast assessment, the performance of the switch paths from input port 1 to all output ports and from all input ports to output port 1 are measured. This choice of paths allows the waveguide splitter at port 1 and the waveguide combiners at output port 1 to be fully tested. In addition, the choice of paths allows for the shortest path (1 to 1) and longest path (4 to 1, 1 to 4) to be evaluated. The switch input and output SOAs are biased at 150mA and 320mA respectively. The middle gating SOAs for the seven paths are biased between 35mA to 70mA to achieve an unsaturated fibre-to-fibre gain of 0dB, with a coupling loss of 3dB per facet.

The wide 3dB gain bandwidth of 30 nm allows the switch to be assessed for potential WDM applications. In this part of the study therefore, eight de-correlated $2^{31}-1$ PRBS 10Gbit/s channels, at wavelengths between 1548.5nm to 1554.2nm with 0.8nm channel spacing, are used. Arrayed waveguide gratings are used as a multiplexer at the transmitter and as a band passed filter before the receiver. Polarization controllers and isolators are used to control the signal polarization state into the switch and to reduce back-reflections within the system. An optical attenuator is used at the transmitter output to vary the input power range into the device for bit error rate measurements. The power penalties incurred by the switch are compared with the 'back-to-back' case with the switch bypassed at 1552.5nm. Minimum power penalties between 0.3dB and 1.6dB at a BER of 10^{-9} are recorded. All paths have a 6dB Input Power Dynamic Range (IPDR) for power penalties below 2dB; with some paths provide IPDRs up to 10dB.

The low power penalty and wide dynamic range shows the potential for the use of the 4×4 switch in multi-stage switch architectures. Large switch architectures can be built using 4×4 base switching elements through using the 3-stage hybrid Clos-Tree architecture [5]. A layout of a 3-stage architecture 16×16 switch using only 12 4×4 switches is shown in Figure 2. Cascading of three 4×4 switches therefore represents a partly populated 16×16 switch, and allows the assessment of its feasibility. In order to evaluate the dynamic performance, single and multichannel transmission through three 4×4 switch cascades is carried out. The test bed is shown in Figure 3. For single wavelength evaluation, a channel at 1552.5nm has been used and for multi-channel measurements, the same wavelength channels as above are used, which gives the 16×16 switch a total capacity of 1.28Tbits/s. All the switches are biased to provide 0dB fibre-to-fibre gain as in previous measurements. The loss between each cascade stage is 2dB and includes three dominant contributions: 0.8dB for the power tap, 0.8dB for the isolator and 0.4dB for the polarization controller. Lensed fibres are used to couple light between the monolithic circuits and the fibre to waveguide coupling loss is measured to be 3-5dB per facet. Because the coupling fibre lenses used for the third switch has a 2dB greater loss than in other cases, an EFDA (not shown in the figure) is used after the second stage to compensate for the loss in the 8 wavelength experiment. The eye diagrams, taken after the isolators of each stage, are also shown.

Fig. 2. Schematic of 3-stage 16×16 switch architecture based on 4×4 switch elements

Fig. 3. Whole test bed schematic for switch performance investigation. The red dashes show the path for 'back-to-back' measurement, which the switches and lensed fibres are bypassed. The Eye diagram is also shown for the outputs from each switch for single switch performance and multiple switch cascades.

The IPDRs for both the single wavelength and for 8 channel experiments are shown in Figure 4. With additional cascades, the IPDR of the switch narrows and the penalty floor increases. This is caused by the accumulation of ASE noise and non-linear distortion after each 4×4 switch stage. For single wavelength transmission, a 6.5dB IPDR

is measured for power penalty below 3dB after three cascaded 4×4 switches, and lowest penalty observed being 1.7dB. The penalty degradation is more pronounced for the 8 channels transmission, where a minimum of 3.4dB power penalty and an IPDR below 4dB penalty of 6dB are observed after three cascades.

Fig. 4. Degradation of signal quality with increasing number of switch cascades. Power penalty as a function of on-fibre input power is plotted for 1 wavelength channel (left) and 8 wavelength channels (right) for 1, 2 and 3 switch cascades.

4. Discussion

A greater integration level could enhance overall performance of switches due to less fibre to waveguide coupling loss, reduction of facet reflection and better reliability. Therefore, to build large switching matrices, integration is essential. In the cascaded experiment, each stage has an inter-stage loss of 8-10dB: 6-8 dB from two fiber-to-waveguide coupling losses and 2dB for isolator, polarizer controller and tap loss. Because the coupling and component losses would not be present in an integrated form, larger integrated switches may be feasible. For example, to build a 64×64 switch, eight 4×4 switches can be placed in parallel with 2 splitters and 2 combiners before and after them to generate a middle 16×16 switch. Hence one could form a 3-stage Hybrid Clos-Tree architecture using 64 4×4 switches in total. Assuming that the active-passive integration would not introduce extra power penalties between stages, and the integrated passive splitter and combiner loss is 3.5dB, a 64×64 switch using the hybrid Clos-Tree architecture would introduce a total of 7dB inter-stage loss. On the basis of the measurements in this paper, construction of an integrated 64×64 switch would therefore be feasible. An improved performance could be anticipated for greater integrated being used smaller switch sizes of 16×16 and 32×32 owing to the lower inter-stage losses which would allow for a greater degree of current control for performance optimization [6].

5. Conclusion

The first high capacity multi-stage assessment of a monolithic integrated 4×4 QW SOA switch is demonstrated, showing this compact lossless switch has a great potential for high speed switching applications. After cascading three switches, routing is achieved of $8\lambda \times 10\text{Gb/s}$ signals with an IPDR of $>6\text{dB}$ at power penalties $<4\text{dB}$. All switches exhibit a 0dB fibre-to-fibre unsaturated gain. This illustrates the potential for these switches to enable a 16×16 switch network based on a 3-stage network of integrated 4×4 switches or a higher port count integrated switch.

6. Acknowledgements

The authors would like to acknowledge Mark Thompson for technical assistance. The UK EPSRC is acknowledged for funding under the HIPNet project as is the European Union for funding the FP7 NoE BONE.

7. References

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