Calibration and Debugging of Multi-Step Analog to Digital Converters

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Abstract

This paper reports a new approach for debugging of the analog to digital converters based on process monitoring and extended design-for-test implementation. The circuit is re-configured in such a way that all sub-blocks are analysed and tested for their full input range allowing full observability and controllability of the analog to digital converter. To set initial data, estimate the parameter update and to guide the test, dedicated monitors have been designed. Additionally, the second presented algorithm allow circuit calibration without explicit need for any dedicated test signal nor requires a part of the conversion time. It works continuously and with every signal applied to the ADC.

Keywords: multi-step ADC, debugging, design-for-test, calibration

1 Introduction

CMOS technologies move steadily toward finer geometries, which provide higher digital capacity, lower dynamic power consumption and smaller area, which results in integration of whole systems, or large parts of systems, on the same chip. With increased system complexity and reduced access to internal nodes, the task of properly testing these devices is becoming a major bottleneck. Additionally, the large number of parameters required to fully specify the performance of mixed-signal circuits and the presence of both analog and digital signals in these circuits make the testing expensive and a time consuming task. Particularly for nanometre CMOS ICs, the large number of metal layers with increasing metal densities, prevents physical probing of the signals for debug purposes. Since parameter variations depend on unforeseen operational conditions, chips may fail despite they pass standard test procedures.

Faults in each one of the components in multi-step ADC affect differently [1] its transfer function. Analyzing and exploring this property form the basis of our approach. The proposed design-for-test (DfT) approach, which is extension on [2], permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range allowing full observability and controllability of the device under test. To estimate performance errors, we employed the steepest-descent method (SDM) algorithm [3], since it requires a small number of operations per iteration and does not require a correlation function calculation nor matrix inversions. Additionally, to enhance observation of important design and technology parameters, such as temperature, threshold voltage, etc., and to update the algorithm parameter estimation, dedicated monitors are embedded within the functional cores [4-5]. To calibrate the accuracy-limiting components, modification on digital offset extraction and analog compensation algorithm [6-8] has been evaluated and implemented.

2 Multi-Step ADC

The input signal is sampled by a three-times interleaved sample-and-hold (S/H), eliminating the need for re-sampling of the signal after each quantization stage. As shown in Figure 1, the S/H splits and buffers the analogue delay line sampled signal that is then fed to three A/D converters (ADCs), namely, the Coarse (4 bits), the Middle (4 bits) and the Fine (6 bits).

Figure 1: Block diagram of the Multi-step ADC and test control circuitry

The quantization result of the Coarse A/D converter is used to select the references for the mid quantization in the next clock phase. The selected references are combined with the held input signal in two dual-residue amplifiers, which are offset calibrated. The mid A/D converter quantizes the output signals of these mid-residue amplifiers. The outputs from both

coarse and mid A/D converters are combined in order to select proper references for the fine quantization. These references are combined with the sampled input signal in two, also offset calibrated, dual-residue amplifiers. The amplified residue signals are applied to a fine A/D converter. The test-shell contains all functional control logic, the digital test-bus, a test control block (TCB) to control testability within the ADC and a CTAG isolation chain for digital IO to and from other IP/cores. Further, logic necessary for creating control signals for the analog circuit parts, and for the scan-chains a bypass mechanism, controlled by the TCB, is available.

3 Estimation Method

Even though extensive research [9-12] has been done to estimate the various errors in different ADC architectures, use of DfT and dedicated monitors for analysis of multi-step ADC to update static parameter estimates have been negligible. The static parameters are determined by the analog errors in various ADC components and therefore, a major challenge in ADC test is to estimate the contribution of those individual errors to the overall ADC linearity parameters. If timing errors are not considered, the primary error sources present in a multi-step ADC are systematic decision stage offset errors (λ), stage gain errors (η), and errors in the internal reference voltages (γ). Each of the three types of errors defined above is the combined result of two physical effects: noise, which includes charge injection noise in analog switches, thermal, shot and flicker noise, and noise coupled from digital circuitry (via crosstalk or substrate), and on-chip process parameter variation, e.g. device mismatch. Systematic decision stage offset (λ) moves the decision levels, while the stage gain error (η) scales the total range of residue signal and causes an error in the analog input to the next stage when applied to any nonzero residue. The residue signal V_{res} is incorrect exactly by the amount of the nonlinearity caused by errors in the internal reference voltages γ

$$V_{res} = \eta V_{in} - (s-1)\gamma V_{ref} - \lambda V_{offset} \quad (1)$$

where s is the observed stage. To obtain a digital representation of (1) each term is divided with V_{ref}

$$D_{out} = \eta D_{in} - (s-1)\gamma - \lambda D_{os} \quad (2)$$

where $D_{in} = V_{in}/V_{ref}$, $D_{out} = V_{res}/V_{ref}$, and $D_{os} = V_{offset}/V_{ref}$. By denoting the k th stage input voltage as $D_{in,k} = V_{in,k}/V_{ref}$, the k th stage output voltage as $D_{out,k} = V_{res,k}/V_{ref}$, and the k th stage decision D_k , a recursive relationship when (2) is applied to each stage in sequence becomes

$$\begin{aligned} D_{out} = D_{out,3} &= \{[\dots]\eta_2 - (D_2 - 1)\gamma_2 - \lambda_2 D_{os,2}\}\eta_3 \\ &\quad - (D_3 - 1)\gamma_3 - \lambda_3 D_{os,3} = \\ &= D_{in,N}\eta_N \dots \eta_1 - (D_3 - 1)\gamma_3 - \lambda_3 D_{os,3} \end{aligned} \quad (3)$$

Such a model is useful both to economically generate an adaptive filtering algorithm look-up table for error estimation and fault isolation. By forcing the input signals to each stage, we control the input to a filter. The desired output, D_{out} is collected from the back-end ADC and subtracted from the corresponding nominal value. This desired response is then supplied to filter for processing. Although in estimation theory several methods are available to estimate the desired response $D_{out}(t)$, the steepest-descent method (SDM) algorithm [3] offers the smallest number of operations per iteration and does not require correlation function calculation nor matrix inversions. Essentially, the SDM algorithm involves creation of an estimation error, e , by comparing the estimated output $D'_{out}(t)$ to a desired response $D_{out}(t)$ and the automatic adjustment of the input weights $(W')^T = [\eta', \gamma', \lambda']$ in accordance with the estimation error e as shown in Algorithm 1. On-chip temperature information [5] and statistical data extracted through the die-level process monitors (DLPM) measurements [6] allows us to characterize current process variability conditions of parameters of interest, and to provide the estimates W' with an initial value.

Algorithm 1

Initialization

- Initialize the input vector $D_{in}(0)$
- Force the inputs and collect the desired output $D_{out}(0)$
- Measure and set the initial value of the weights $W'(0)$
- Initialize the steepest descent update step $\mu=1$
- Initialize the forgetting factor ζ

Data collection

- Collect N samples from the DLPM and temperature sensors
- Collect N samples from the AD converter

Update parameter estimate

1. Update the input vector $D_{in}(t+1)$ based on current available $W(t)$
 2. Calculate the error estimate $W'(t)$
 3. Generate the output estimate $D'_{out}(t) = D_{in}(t) \times W'(t)$
 4. Calculate the estimation error $e(t) = D'_{out}(t) - D_{out}(t)$
 5. Calculate the error estimate $W'(t+1) = W'(t) - \mu \times D_{in}(t) \times e(t)$
 6. If $W'(t+1) > W'(t)$ decrease step size μ and repeat step 5
 7. Increase the iteration index, t and repeat steps 1-6 for best estimate
 8. Denote the final value of W' by W'_t
 9. If temperature changes update W' with new estimate $W'(t+1) = \zeta W'(t) + (1-\zeta)W^0(t+1)$
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4 Calibration

The dominant error contributing components in the signal path before gain is applied are the S/H, the reference ladder, the switches in the switch unit and the offset on the residue amplifiers. Since sufficient power is spend to meet the noise and linearity requirements of the S/H and matching of the reference resistors is adequate for 12-bit level, the offset on the residue amplifiers is now the only accuracy-limiting component. Therefore, to maintain speed in the residue amplifiers while accomplishing 12-bit linearity requirement, offset calibration has to be applied. As offset is an analogue property, a calibration DAC is used to compensate for the offset

[illegible]

The different effect of the common and the differential offset extractors can be seen as the adders. A change caused by the common offset extractor gives both calibration DAC values a step of the same sign, while a change caused by the differential offset extractor gives a step of opposite sign. These calibration DACs close the compensation loop. Thereby the offset in the residue amplifiers is removed. Since the adjustment of the compensation values is with ± 1 at a time, it can take quite a while before the end value is reached. For instance, taking 256 times 216 samples will take at 80 Ms/s at least 200 ms. To avoid this, a quick calibration algorithm has been build in as shown in Figure 3.

When this mode is enabled, the inputs of the residual amplifiers will be shorted together. As a result the output will show the offset only, which will be fed to a comparator that compares with the value 0. By setting the bits from MSB to LSB of the compensation DACs and keeping/resetting the values depended of the comparator output, it takes only nine small cycles of eight clocks per DAC to calibrate. The quick calibration results are taken over by the normal (slow) calibration loop, where the convert signal steers the multiplexer that selects between an update from the quick or the normal loop. Note that for the Fine ADC the number of samples used for averaging is increased by a factor of eight.

A prototype layout of the multi-step ADC is shown in Figure 4. The ADC converter with dedicated sensors is fabricated in standard single poly, five metal 0.09- μm CMOS with the core area of 1.4 mm^2 . The ADC operates at 1.2 V supply voltage and dissipates 100 mW (without output buffers). The ADC has no missing codes and the differential nonlinearity (DNL) remains within $\pm 1\text{LSB}$. One temperature sensor (located at the top right corner) and a total of 125 DLPMS, which are divided into specific groups, have been placed in and around the partitioned multi-step ADC. Each group of sensors target specific error source. To evaluate the two proposed algorithms consider the test results shown in Figures 5-9. λ , η , and γ are generated randomly, so that the relative errors are uniformly distributed in the interval [-0.1,0.1]. At first, update μ was set to 1/4 to speed up the algorithm, and then μ equal to 1/64 after 1000 iteration times to improve the accuracy.

Although the accuracy increase quite slowly with the amount of data, evaluated ADC, however, use very high sample rates (50 MS/s) so some million samples are collected in less than second.

With the use of dedicated monitors, which exploit knowledge of the circuit structure and the specific defect mechanisms, we facilitate the readout of local (within the core) performance parameters as well as the global distribution of these parameters at the cost of at maximum 10% area overhead. The flexibility of the concept allows the system to be easily extended with a variety of other performance monitors. The implemented design-for-test approach permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range. Employed algorithm for diagnostic analysis offers the small number of operations per iteration and does not require correlation function calculation nor matrix inversions. The presented calibration algorithm does not need any dedicated test signal and does not require a part of the conversion time. It works continuously and with every signal applied to the ADC.

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Figure 5: Mean-square error for two million samples. The quality criterion adopted is the mean-squared error criterion, mainly because of the possibilities to assign the weights.

Figure 6: DNL curve before calibration. Defects result mainly from errors in fine ADC.

Figure 7: DNL curve after calibration.

Figure 8: INL curve before calibration. The INL is mainly caused by the ladder non-linearity. Errors affecting the reference divider introduce transition position errors since the transitions do not coincide with the range of the next stage.

Figure 9: INL curve after calibration.