Demonstration of Label-Rewriting using 1 x 4 All-Optical Packet Switch employing Optical Processing of Scalable In-Band Labels

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Abstract: We demonstrate label-rewriting function using 1x4 all-optical packet-switch that utilizes a highly scalable and asynchronous label processor. Results show that labels are successfully exchanged and the process causes only 0.5dB power-penalty and error-free operation at 160Gb/s.

Keywords: Optical packet switching, Optical processing

1. Introduction

All-optical packet switching is expected to be a promising candidate to solve the mismatch between the fiber bandwidth and router forwarding capacity at bit-rate where electronics is too slow to directly process the data [1]. In an all-optical packet switch, the packets are routed based on address information that is encoded by attached labels.

A key issue in the implementation of all-optical packet switch is to reduce the total number of optical switches required for the realization of the packet switched cross-connect. For instance, if 1x2 optical switch is used, the total of optical switches is proportional to N² because the number of optical switches needed at each fiber input in a NxN WDM switching node is N², where N is the number of the input port. However, if 1xN optical switch is available, the total number of optical switches required for the cross-connect would be proportional to N and thus drastically decreased. To implement 1xN optical packet switch, it is essential to realize a highly scalable label processing technique that can process N labels in parallel.

Recently, we reported a 1x4 optical packet switch based on a new scalable label processor for encoded in-band labelling addresses [2]. In [2], we have demonstrated all-optical label erasing and processing. To accomplish the label swapping technique, however, a label-rewriting function that provides a new label from the old one needs to be realized.

In this paper, we demonstrate a label-rewriting function capable of providing a new label based on the old input label. The scheme can be built using a similar set-up employed for the label processor demonstrated in [2]. The performance of the label-rewriting function was evaluated by the power penalty at each node of two cascaded nodes.

2. System Operation

Figure 1 shows the experiment setup for label-rewriting. Packet payload is generated by time-multiplexing a 40Gb/s return-to-zero data-stream carrying 2^31-1 PRBS data at λ₁=1548.9nm up to 160Gb/s data-stream using a passive fiber-based pulse interleaver. Each bit has duration of 1.6ps making the 20dB bandwidth of the payload to be 5nm. The resulting packet payload consists of a 250 ns data burst. The packet-to-packet guard time is 10 ns, making the packet repetition rate 260 ns.

We encode addresses by using two labels with different in-band wavelength, which enables to encode 4 different addresses. The in-band label has the advantage that the labels can be extracted by passive wavelength filtering, which simplifying the label processing. Moreover, using a label that has the same time-duration as the packet-payload makes the use of an optical flip-flop redundant. In the experiment, we used two labels with the wavelengths of λ₁=1551.9 nm and λ₂=1552.5 nm which are within the 20-dB optical bandwidth of the packet-payload.

The label re-writer consists of an all-optical label extractor (used in common with the label processor), an all-optical new label generator that has the same structure as the label processor in [2] and a passive optical coupler. The input packets to the packet switch are firstly processed by the label extractor. The label extractor consists of two fiber (reflective) Bragg gratings (FBG) with a 3dB bandwidth of 0.12 nm and 0.432nm centered at λ₁ and λ₂ respectively. While the packets pass along the label extractor, the label that fits with the wavelength of each FBG is taken (reflected) out. After the label extraction, the old labels are erased and the payload is fed into the wavelength converter [2].

The new label generator receives the CW-signals as inputs, which represents the new labels. The wavelengths of the CW-signals are set to be in-band with the switched payload (the central wavelength of the payload is set by the label processor[2]). For a given old labels combination, the control wavelength is provided by the label processor, and the new label is provided by the label generator. As an example, if packet with labels ‘0 1’ enters the packet switch, the label processor produces a cw-signal at 1560.8 nm (at which the payload is converted) and the label rewriter produces a new label ‘1 0’, which is represented by the cw-signal at 1559 nm, that will be attached to the converted payload.
Each of the extracted labels is fed into each of the MZI-SOAs of the new label generator. The MZI-SOA acts as a fast wavelength selective switch. As shown in Fig.1, CW signals at (\(\lambda_1, \lambda_2, \lambda_3\)) are applied to the port 1 and 2 of MZI-SOA1, respectively. At output of MZI-SOA1, the signals \((\lambda_1, \lambda_2, \lambda_3)\) appears. However, if there is the label \((\lambda_i)\) at the control input of the MZI-SOA1, the signal \((\lambda_i)\) comes out. The AWG and the 2x1 couplers are used to separate the pair of CW-signals and feed them to the two input ports of MZI-SOA2. According to the label \((\lambda_{i2})\), the MZI-SOA2 will give a distinct set of new labels at the output. This set of new labels is then combined with the 160Gbs wavelength converted payload and composed of a new packet.

3. Experiment and Results

The experimental setup of the label-rewriting demonstration employing two-bit labels is illustrated in Fig.1. We processed four packets with two-bit labels with pattern of ‘0 0’, ‘0 1’, ‘1 0’, ‘1 1’ to cover all possible combinations. The label bits extracted by the label extractor are shown in Fig.2 (a, b). Figure 3(b) shows the spectrum of the payload signal after label extraction. As compared with Fig. 3(a), the label was erased. Based on the two-bit labels, the new label generator gave four sets of new labels shown in Fig.2 (c-f) where ‘0 1’ (old) \(\rightarrow\) ‘1 0’ (new), (c) represented by ch 23; ‘0 0’ \(\rightarrow\) ‘1 1’, (d, e) represented by ch35, ch39; ‘1 0’ \(\rightarrow\) ‘0 0’, no outputs; ‘1 1’ \(\rightarrow\) ‘0 1’, (f) represented by ch 41. New labels from the label generator were combined with the 160Gbs wavelength converted payload. The spectrum of the converted payload with new labels is shown in Fig. 3(c). To emulate the output of the label processor in [2], CW signal at 1560.6nm was used. The converted payload and new labels are processed in node2. At node2 the quality of the payload is evaluated after the label extractor. (See also the spectrum of Fig.3(d))

Figure 4 shows the BER performance at different position of the switch. The label extractor produces a penalty of less than 0.5dB. After the wavelength conversion, error-free operation was obtained with 5.5 ~ 7dB of penalty compared to the input payload, and 1.5dB ~ 3dB of additional penalty as compared with the back-to-back of 160Gbs wavelength conversion. The extra penalty can be ascribed to the pulse broadening after the label extractor which affects the performance of the wavelength conversion. As shown in figure, the label-rewriting function doesn’t cause any critical power penalty.

5. Conclusion

In this paper, we demonstrate label-rewriting function using a high scalable and asynchronous label processing structure. In the experiment, the labels are successfully exchanged and the process causes 0.5dB of power penalty, achieving error-free operation at 160Gb/s. We believe that the new structure is promising as a fundamental building block for future large-scale optical packet switching.

6. References
