Control of Grid-Interactive Inverters as Used in Small Distributed Generators

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Abstract—Small distributed generation (DG) systems provide standby service during utility outages and, when operated during peak load hours, potentially reduce energy costs. The connection of a generation system to the utility grid requires a robust phase locked loop (PLL) and continuous detection of utility grid status (such as outage, over-/under-voltage and over-/under-frequency). This paper details a flexible control strategy to operate a small/micro single-phase DG in both stand-alone and grid-connected modes. The described system is effectively an extended line-interactive uninterruptible power supply (UPS). In particular, a high-performance PLL for single-phase inverters is proposed. The PLL uses a transport delay method to generate a virtual quadrature signal, thereby emulating a balanced three-phase system. Furthermore, an orthogonal filter is incorporated to improve the PLL performance when the grid voltage is distorted. To achieve zero steady-state error and to implement selective harmonic compensation, resonant controllers are proposed, for both the voltage regulation in stand-alone control mode and the current regulation in grid-connected control mode. Simulation and experimental results from a 3.5 kW prototype with a fuel cell as the primary source are included to prove the effectiveness of the proposed methods.

I. INTRODUCTION

Most sustainable energy sources supply energy in the form of electrical power. Distributed generation (DG) systems are often connected to the utility grid through power electronic converters. A grid-connected inverter provides the necessary interface of the DG to the phase, frequency and amplitude of the grid voltage, and disconnects the system from the grid when islanding. Such a DG system can be designed to operate in both stand-alone and grid-connected modes flexibly according to grid conditions [1], [2]. When the utility grid is not available or the utility power is accidentally lost, the DG is used as an on-site power or standby emergency power service, effectively being an extended uninterruptible power supply (UPS) that is capable of providing long-term energy supply.

An experimental system [3] is shown in Fig. 1. A fuel cell is used as the primary source and a supercapacitor is employed as the storage. The power conditioning unit of the system consists of a grid-interfacing inverter and a three-port bidirectional dc-dc converter [4] that interfaces three power ports, namely the fuel cell, supercapacitor and inverter [5]. The system operates in grid-interactive mode. By taking advantage of the transient storage capability offered by the

supercapacitor, the function of active power filtering can be integrated into the system. The inverter is simultaneously operated as a shunt active filter and compensates for the reactive and harmonic current demanded by local loads [1]. The initial implementation of the system is at a power level typical for home applications (maximum 3.5 kW). Therefore a single-phase version is considered throughout the paper. With a few modifications, it is possible to extend the system to a higher power level using a three-phase configuration.

The main topics of this paper are the control of the pulse-width modulated (PWM) inverter and the grid interfacing of the system. Since the system should be able to operate in both stand-alone and grid-connected modes according to the grid conditions, the control design is somewhat challenging.

It is shown that by using resonant controllers [6] for both the current regulation in grid-connected control mode and the voltage regulation in stand-alone control mode, zero steady-state error and fast transient response can be achieved. Resonant controllers are also used to implement selective harmonic compensation [7]. For connecting the DG system to the grid, a high-performance phase locked loop (PLL) structure for single-phase systems is presented. The PLL structure is implemented with a transport delay and an orthogonal filter. The transport delay is used to generate a virtual quadrature signal [8] and the orthogonal filter, which has been proposed for three-phase systems [9] (also referred as multivariable filter), is employed for improving the PLL performance when the grid voltage is distorted. The operation of the system requires a real-time detection of grid status (such as outage, over-/under-voltage and over-/under-frequency). An automatic and smooth transition between the two operating modes can be achieved by using a static transfer switch (STS) and ramping up the reference signal in a few consecutive grid cycles [10]. All the proposed control methods have been developed and implemented with a digital signal processor (DSP).

This paper is presented as follows. Section II describes the inverter control in stand-alone mode of operation. Then, control methods for grid-connected operating mode including the PLL design and current regulation of the inverter are explained in Section III. Practical issues like grid status detection are addressed in Section IV. Simulation and measurement results are provided in Section V to verify the control methods. Finally, conclusions are drawn in Section VI.

Fig. 1. A fuel cell DG system operating in both stand-alone and grid-connected modes, where L_f and C_f form the inverter output filter, Z_L is the grid impedance, STS is a triac for connecting the DG to the grid, and POC stands for the point of connection.

Fig. 2. Inverter in stand-alone mode of operation.

II. CONTROL IN STAND-ALONE MODE OF OPERATION

During a grid outage the DG operates in stand-alone mode (shown in Fig. 2) to supply uninterrupted power for local critical loads. The system is disconnected from the grid by opening the STS. In this operating mode, the inverter voltage must be controlled and the control of the system is focused on the quality of the output voltage. Many control strategies have been explored in the literature [11]. The most commonly reported scheme is the two-loop control strategy where the inner current feedback loop provides fast compensation for input supply disturbances and the outer voltage loop generates the reference for the inner current control loop. The feedback signal for the inner current loop can be either the filter capacitor current or the filter inductor current. Furthermore, various disturbance feedforward schemes for decoupling can also be incorporated to improve steady-state tracking performance. Capacitor current feedback is preferred because of its inherent ability to forecast the change of the output voltage ($i_C = C_f dv_O/dt$, see Fig. 1). The capacitor current changes instantaneously with the load current change, irrespective of the inductor current, and therefore provides a rapid control action to correct the output voltage [11].

The combination of a proportional-resonant (PR) controller with capacitor current feedback is shown to be superior in achieving perfect reference tracking at the fundamental

Fig. 3. Bode plot of the proportional resonant (PR) controller.

frequency [11]. The transfer function of the PR controller can be written as [6]:

$$G_v(s) = K_P + \frac{2K_I\omega_c s}{s^2 + 2\omega_c s + \omega_1^2} \quad (1)$$

where K_P and K_I are the proportional and integral gain, and ω_1 and ω_c are the fundamental frequency and integrator low frequency cutoff, respectively. The PR controller is mathematically equivalent to a synchronous frame PI controller. It resonates at ω_1 and thus has a very high gain around ω_1 . The Bode plot of the PR controller is shown in Fig. 3, where $K_P = 1$, $K_I = 20$, $\omega_c = 10$ rad/s, and $\omega_1 = 314$ rad/s.

There are obvious advantages of using a PR controller instead of a PI one. A PI controller introduces infinite gain at dc. Therefore the dc offset in the sampling and ADC circuit and/or the numerical error caused by the limited word-size of the DSP will be accumulated over time and eventually leads to saturation of the PI output. In some cases, PI-type controllers with an ideal integrator cannot function in real setups. To solve this problem, the ideal integrator can be approximated by a low-pass filter with a limited gain. Alternatively, a high-pass

Fig. 4. Block diagram of the inverter control in stand-alone operating mode with outer capacitor current proportional-resonant (PR) control and inner inductor current proportional (P) control, where K_{PWM} is the inverter gain, m is the modulation index, r_L is the resistance of the filter inductor, and Z_{LD} is the load impedance.

filter with a suitably low cutoff frequency can be employed to filter out the dc components. With the PR controller the system open-loop gain at dc is low, while the gain at the resonant frequency can be very high. Obviously, the effect of offset and noise in the ADC sampling and conversion circuit can be ignored.

Fig. 4 illustrates the two-loop control structure for the inverter in stand-alone mode of operation. To provide over-current protection, instead of the capacitor current i_C the inductor current i_L and load current i_{LD} are measured as the feedback signals. Since the capacitor current is the difference between the inductor current and the load current, this method is equivalent to simple capacitor current feedback control. The PR compensator in the outer voltage regulation loop eliminates the steady-state error. The inner current loop is implemented with proportional control. In addition, an output voltage disturbance feedforward term is added to the output of the current controller to improve the system dynamics.

III. CONTROL IN GRID-CONNECTED MODE OF OPERATION

When the grid voltage is normal, the inverter is tied to the grid (the STS is closed) as shown in Fig. 5. The inverter is current controlled. In this mode of operation, the DG system not only injects real power into the POC, but also compensates for the reactive and harmonic current demanded by local loads [1]. The equivalent model of the system and operating waveforms are illustrated in Fig. 6. The control objective is to minimize the harmonics of the current injected into or drawn from the grid.

A. High-Performance PLL Design

In grid-connected mode of operation, a fast and accurate PLL method is essential because the generation of the current reference is based on the output of the PLL. As a result, the performance of the whole system is largely influenced by the effectiveness of the PLL strategy, especially when the grid voltage contains harmonics and could be unbalanced. The synchronous reference frame PLL has been widely used in three-phase systems for its good tracking performance.

In the three-phase system, the grid frequency, phase angle and amplitude, can be easily obtained from the voltage space vector. However, for a single-phase system, acquiring the phase angle information is much more difficult because of

Fig. 5. Inverter in grid-connected mode of operation.

Fig. 6. Equivalent model of the system in grid-connected mode of operation.

the lack of a quadrature signal. The commonly used zero-crossing detection method does not provide instantaneous phase angle information of the grid and is sensitive to multiple zero-crossings caused by noise. Therefore the main issue of designing a single-phase PLL is how to generate the virtual quadrature single and mimic a balanced three-phase system. Among many proposed methods the transport delay method, as suggested in Fig. 7, is believed to be the simplest and most effective one [8]. The input grid voltage is stored in memory and the quadrature component is obtained by accessing the data history with a delay of 1/4 grid cycle ($T/4$). With this estimated quadrature signal, the single-phase system can be treated as a balanced three-phase system and most PLL control strategies for three-phase systems can be applied. The proposed PLL structure for the single-phase situation is shown in Fig. 7, where v_G is the sampled grid voltage, and $\omega_{ff} = 314$ rad/s is the feedforward term (for 50 Hz grid frequency).

Note that a so-called orthogonal filter is included in the PLL structure (also see Fig. 9). It is well known that the performance of the synchronous reference frame PLL is degraded when the grid voltage is distorted, and especially when the voltage is unbalanced. To improve the robustness of the PLL,

Fig. 7. Proposed PLL structure with a transport delay and an orthogonal filter for single-phase systems.

an orthogonal filter can be employed [9]. The following shows the mathematical derivation of this filter.

The stationary equivalent of an integrator in the synchronous reference frame rotating at ω_1 can be expressed as

$$G_I^s(s) = \frac{1}{s - j\omega_1}. \quad (2)$$

The above transfer function is obtained by substituting the integrator's s with $(s - j\omega_1)$. The physical meaning of this transformation is that the frequencies of all quantities in the synchronous reference frame are shifted by ω_1 when transferred to the stationary reference frame. Note that both the input and output are complex variables. Let us now design a unity gain low-pass filter (LPF) for the synchronous reference frame:

$$G_{LP}^e(s) = \frac{\omega_p}{s + \omega_p} \quad (3)$$

where ω_p is the pole frequency of the LPF in the synchronous reference frame and the superscript “e” in G_{LP}^e denotes that the transfer function is expressed in the synchronous frame. Then in the stationary frame, the filter can be expressed as

$$G_{LP}^s(s) = \frac{\omega_p}{(s - j\omega_1) + \omega_p}. \quad (4)$$

where the superscript “s” in G_{LP}^s indicates that the transfer function is expressed in the stationary frame. Rationalizing the denominator yields

$$G_{LP}^s(s) = \frac{\omega_p((s + \omega_p) + j\omega_1)}{(s + \omega_p)^2 + \omega_1^2}. \quad (5)$$

From the above equation, it is obvious that an LPF in the synchronous reference frame is equivalent to a band-pass filter (BPF) in the stationary frame, ω_p corresponding to the half width of the passband. Fig. 8 illustrates the synchronous reference frame LPF and its equivalent in the stationary reference frame. For a space vector, rotating the reference frame effectively changes the rotating frequency of the vector.

The filter cleans the orthogonal voltage signals (a space vector) before they are fed into the PLL block. Therefore

Fig. 8. Synchronous reference frame low-pass filter (LPF) and its equivalent in the stationary reference frame.

Fig. 9. Implementation of the orthogonal filter.

the operation of the PLL is insensitive to disturbances in the grid voltage. Moreover, with the two orthogonal signals, the implementation of the filter is simple. Let v_α and v_β denote the input signals of the filter and $\hat{v}_\alpha$ and $\hat{v}_\beta$ denote the output signals. Then

$$\frac{\hat{v}_\alpha(s) + j\hat{v}_\beta(s)}{v_\alpha(s) + jv_\beta(s)} = G_{LP}^s(s) = \frac{\omega_p}{(s - j\omega_1) + \omega_p}. \quad (6)$$

After some manipulations, the following expressions can be obtained:

$$\begin{aligned} \hat{v}_\alpha(s) &= \frac{1}{s} [\omega_p(v_\alpha(s) - \hat{v}_\alpha(s)) - \omega_1\hat{v}_\beta(s)] \\ \hat{v}_\beta(s) &= \frac{1}{s} [\omega_p(v_\beta(s) - \hat{v}_\beta(s)) + \omega_1\hat{v}_\alpha(s)]. \end{aligned} \quad (7)$$

Fig. 9 is a graphical representation of Eq. (7). Therefore the orthogonal filter expressed by Eq. (4) can be implemented using Fig. 9. As shown, only two integrations and multiplications need to be performed [9].

In summary, with the transport delay method and the orthogonal filter, a high-performance PLL for a single-phase system can be realized.

B. Current Regulation for Single-Phase Inverters

Conventionally, PI-type ramp comparison controllers have been used to regulate the inverter output current, although they have drawbacks such as steady-state error (both magnitude

and phase) and limited disturbance rejection capability. These controllers are usually designed as an analog circuit. With a digital implementation the one sample delay in the feedback loop reduces the phase margin significantly, and thus causes stability problems. Therefore PI type current regulators are, in general, not suitable for digital control of inverter output current.

Again, as in the stand-alone mode of operation, a PR controller similar to (1) can be employed to regulate the inverter current in the grid-connected mode of operation:

$$G_i(s) = K + G_1(s) \quad (8)$$

where K is the proportional gain and $G_1(s)$ is the resonant controller for the fundamental component, given by

$$G_1(s) = \frac{2K_{I1}\omega_{b1}s}{s^2 + 2\omega_{b1}s + \omega_1^2} \quad (9)$$

Although there is a sampling delay, the PR controller has no stability problem. Furthermore, the CPU overhead is less than for the synchronous reference frame controller, because all the computation is performed in the stationary frame and no coordinate transformation is needed. It is possible to regulate the current in the synchronous reference frame as in the three-phase situation, however, at the expense of using more computation power and memory. The controller has good tracking performance for the fundamental signal. It should be noted, however, that the tracking performance decreases at harmonic multiplies since a PR controller only has its largest gain at ω_1 .

Concerning harmonics, DGs are subject to stringent rules. The IEEE 1547 standard allows a maximum of 5% for the current THD with individual limits of 4% for each odd harmonic from 3rd to 9th and 2% for 11th to 15th. It is possible to implement selective harmonic compensation with resonant controllers [7]. Should harmonic compensation be applied to satisfy the standard, then Fig. 10 shows the structure of the current controller, where $G_F(s) = i_O(s)/v_{inv}(s)$; K_{PWM} is the inverter gain; K_F is the feedback gain. For each harmonic, the transfer function of the compensator has the form:

$$G_h(s) = \frac{2K_{Ih}\omega_{bh}s}{s^2 + 2\omega_{bh}s + (h\omega_1)^2} \quad (10)$$

where $h = 3, 5, 7, \dots$, according to the selected harmonics to be compensated. Designers can choose which harmonics have to be compensated according to the situation at hand. To be implementable, the compensators have a passband with certain width ($2\omega_{bh}$). The Bode plot of the open-loop resonant control system for the current regulation with selective harmonic compensation, $G_A(s)$, is shown in Fig. 11, where the gains of the 1st, 3rd, 5th and 7th harmonics are significantly boosted by the resonances at the harmonic frequencies. For comparison, the open-loop transfer function with only the proportional control, $G_B(s)$, is also plotted in Fig. 11. The plotted transfer functions are

$$\begin{aligned} G_A(s) &= K_{PWM}K_F(K + G_1(s) + G_3(s) + G_5(s) + G_7(s)) \\ G_B(s) &= K_{PWM}K_FK \end{aligned} \quad (11)$$

Fig. 10. Structure of the current controller – resonant current controller with selective harmonic compensation.

Fig. 11. Bode plot of the open-loop resonant control system for the current regulation with selective harmonic compensation and only with proportional control.

The parameters used for the Bode plot are $K = 1$, $K_{I1} = K_{I3} = K_{I5} = K_{I7} = 20$, $\omega_{b1} = 10$ rad/s, $\omega_{b3} = \omega_{b5} = \omega_{b7} = 5$ rad/s, $\omega_1 = 314$ rad/s, $K_{PWM} = 400$, and $K_F = 3/64$.

Note that in the actual implementation i_L is measured as the feedback signal instead of i_O , since i_C is very small. i_C can also be compensated for through an injection of capacitive current to the POC. In both operating modes the measured current feedback signals are i_L and i_{LD} , which makes the control easy to implement. A current control strategy for simultaneously operating the DG as an active filter has been proposed in [1]. The main role of the inverter is to inject a constant active power into the POC and compensate for the reactive power of local loads.

IV. GRID STATUS AND ISLANDING DETECTION

To ensure a high-quality power supply for local loads, utility grid status should be monitored continuously in real-time. The grid status includes sensing outage, over-voltage and under-voltage. Outage detection is carried out in every sampling cycle by comparing the instantaneous grid voltage

Fig. 12. Procedures for seamless transitions between the grid-connected and stand-alone modes.

to a preset threshold value. To avoid complications around the zero-crossing region the detection is disabled there. Multiple-time sampling is used to avoid false outage detection caused by noise in the signal. The over-voltage and under-voltage detection are performed by calculating the rms value of the grid voltage in an interval of a grid cycle. This value is compared to a preset value. When an abnormal rms value is seen, the DSP initiates a counter. If the over-voltage or under-voltage persists for a period of, for instance, 10 grid cycles, grid status is identified to be abnormal, and the gating signal of the STS will be shut off immediately. A transition from grid-connected mode to stand-alone mode of operation is initiated. The STS disconnects the system from the grid within half a grid cycle. In order to avoid frequent transitions between the two operation modes, grid voltage sags or swells may not be considered as a grid fault, since most loads may ride it through. Detailed specifications depend on how sensitive the local loads are.

On the other hand, when the grid fault is cleared, a synchronization process shifts the inverter from stand-alone to grid-connected mode of operation. First, the grid voltage is inspected and verified to be within the tolerance limits of the sensitive loads. Once a nominal grid voltage is detected, the control algorithm adjusts the load voltage to match the magnitude and phase of the grid voltage. When the voltages at the both sides of the separation switch STS are locked both in magnitude and phase angle, the STS can be turned on. At the instant of reconnection, the inverter is turned to current control mode. A smooth and seamless transition can be achieved by ramping up the reference signal in a few consecutive grid cycles [10]. The procedures for transitions are illustrated in Fig. 12.

Since utility operators place a high priority on safety and on the reliability of electrical systems, grid interconnection has always been considered as an obstruction to the installation

of DGs. Therefore effective islanding detection is another important issue with DGs. The detection method can be passive (voltage and frequency detection) or active (active frequency drift). It has been suggested by [12] that the current-regulated inverter has a better performance in anti-islanding than the power-angle-regulated inverter. When the grid is de-energized and an islanding condition is detected, the DSP opens the STS and separates the DG from the grid.

V. SIMULATION AND EXPERIMENTAL RESULTS

A prototype rated at 3.5 kW maximum power (according to the regulation for the maximum allowed single-phase power) was constructed. All the control was implemented with a TMS320F2808 DSP from Texas Instruments and the inverter was operated at 20 kHz switching frequency. Table I lists the inverter design parameters.

TABLE I
INVERTER DESIGN PARAMETERS FOR SIMULATION AND EXPERIMENT

Description	Symbol	Value
Dc-link voltage	V_{DL}	400 V
Ac output voltage	v_O	230 V rms
Ac output frequency	f_O	50 Hz
Maximum output power	P_O	3.5 kW
Switching frequency	f_s	20 kHz
Filter inductor	L_f	2 mH
Filter capacitor	C_f	10 μ F

A. Operation of the PLL

The PR controller and the PLL strategy were investigated with Matlab/Simulink for various situations. For the proposed PLL structure, Fig. 13(a) shows the response to a 45° phase jump initiated at 0.5 s, and Fig. 13(b) demonstrates the operation of the PLL with distorted grid voltage, showing that the output of the PLL is locked to the fundamental component of the input signal. The experimental results are presented in Fig. 14. As shown in Fig. 14(a), having detected the normal grid status, the inverter starts the procedure to lock the output to the grid when the grid is re-energized. Furthermore, Fig. 14(b) displays the measured results of the PLL operation when the grid voltage contains harmonics (3rd, 5th and 7th, each 10% of the fundamental component). The grid voltage was produced by a 15 kVA grid simulator from SpitzenBerger + Spies (Model: DM 15000 / PAS, three-phase mains simulation system consisting of three 5 kVA four-quadrant linear amplifiers).

B. Inverter Operation in Stand-Alone Mode

The regulation of the output voltage in stand-alone mode of operation is shown in Fig. 15, where a resistive load was used. Furthermore, Fig. 16 presents the measurement results for the regulation of the output voltage with a diode rectifier load. In both cases the output voltage is well regulated with low distortion. The noise in the measured signals is due to the interferences in the long measuring cable.

Fig. 13. PLL simulation results: (a) response to a 45° step change in phase and (b) performance under distorted input.

Fig. 14. PLL experimental results, showing (a) locking the phase to the grid voltage when the grid is re-energized, and (b) operation of the PLL under distorted grid voltage.

Fig. 15. Measurement results of the output voltage and inductor current in stand-alone mode of operation with a resistive load.

Fig. 16. Measurement results of the output voltage and inductor current in stand-alone mode of operation with a diode rectifier load.

Fig. 17. Simulation results of inverter operation in grid-connected mode with a diode rectifier load.

C. Inverter Operation in Grid-Connected Mode

Simulation results for grid-connected mode of operation are presented in Fig. 17, showing that the inverter supplies the reactive and harmonic current demand of the local load (a diode rectifier) while it injects real power, and that the grid current is an in-phase sinusoidal current.

The experimental results are shown in Fig. 18. A diode rectifier was used as the local load. The inverter compensates for the reactive and harmonic current and injects active current into the grid. Good correlation is found between the simulation and measurement results (compare Fig. 17 with Fig. 18).

For comparison, Fig. 19 displays the waveform when the selective harmonic compensation is not implemented, showing a more distorted waveform of the current (i_G). The FFT results of the current i_G are given in Fig. 20 (with selective harmonic compensation) and Fig. 21 (without harmonic control). As can be seen, the low frequency harmonics (3rd, 5th and 7th) are reduced significantly with selective harmonic control.

VI. CONCLUSIONS

In this paper, detailed control methods for operating a small single-phase DG in both stand-alone and grid-connected modes have been presented. It has been shown that a high-performance PLL for a single-phase inverter can be realized by means of a transport delay which generates a virtual quadrature signal, thereby emulating a balanced three-phase system.

Fig. 18. Measurement results of inverter operation in grid-connected mode with selective harmonic compensation (3rd, 5th and 7th), showing the compensation of the harmonics of the local load (a diode rectifier) and injection of active current to the grid.

Fig. 19. Measurement results of inverter operation in grid-connected mode without selective harmonic compensation.

Furthermore, an easy-to-implement orthogonal filter enhances the PLL performance when the grid voltage is distorted. To achieve zero steady-state error for both the voltage regulation in stand-alone mode and current regulation in grid-connected mode of operation, and to implement selective harmonic compensation, resonant controllers are used. Additionally, the procedures for detecting the grid status and managing the transition between the two operating modes were presented. The effectiveness of the presented methods are proved by the simulation and experimental results from a 3.5 kW prototype.

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Fig. 20. FFT results of the current injected into the grid, i_G , with selective harmonic compensation (3rd, 5th and 7th) (also see i_G in Fig. 18).

Fig. 21. FFT results of the current injected into the grid, i_G , without harmonic control (also see i_G in Fig. 19).

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