A Novel Interpolation Approach for Reducing Clock-Rate in Multilevel Decision Feedback Equalization Detectors

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Abstract—The multilevel decision feedback equalization (MxDFE) family of detectors provides excellent performance over (1, 7)-coded magnetic recording channels, while being simple in structure. However, the reduced code-rate of 2/3 increases the channel data rate by 50% compared to the user data rate. Although this is not a problem for the write heads because of the reduced bandwidth of the (1, 7) writing signal [compared with (0, k) codes], it becomes an issue at the detector side for high-data-rate applications. We propose a novel interpolation approach for reducing the detector clock rate. Performance simulations of MDFE and M2DFE detectors, carried out over different user densities, channel models, and equalizer configurations, show that the proposed scheme can reduce the detector clock rate to the user rate with negligible impact on performance. We also present a timing recovery scheme for acquisition and tracking of the reduced-rate clock.

Index Terms—Clock-rate reduction, interpolation, magnetic recording, multilevel decision feedback equalization, timing recovery.

I. INTRODUCTION

IN ANY data storage application, the two important commodities in demand are recording density and data-rate. The increasing trends in density and data-rate raise the following two challenges: 1) combating the channel distortions that originate at high recording densities, and 2) simplifying the detector design to suit high data-rate implementation. With increase in density, the artifacts such as media noise, partial erasure, and nonlinear transition shifts increase due to decrease in the spacing between nearby transitions [1]. With increase in data-rate, bandwidth limitations of the write-path begin to manifest in the form of nonlinear shifts in the positions of written transitions on the medium [2]. Further, at high data-rates, implementation of the detector, whose complexity tends to increase

for high performance, becomes a serious concern. The multilevel decision feedback equalization (MxDFE) family of detectors (viz., MDFE, M2DFE, M3DFE, and M4DFE), which uses the run-length-limited (RLL) rate 2/3 (1, 7) code, has been shown to offer viable solutions to overcome most of these problems [3]–[5], [13]. Because the minimum spacing between transitions is increased by the $d = 1$ code constraint, the transition density dependent artifacts are less serious in (1, 7)-coded channels compared with (0, k)-coded channels. Further, the bandwidth of the (1, 7) writing signal is significantly smaller, thus, making it writing friendly [3]. Moreover, the design of MxDFE detectors exploiting the $d = 1$ constraint and incorporating certain novel and advanced features helps to attain performance that is close to optimum [5], [13].

In this paper, we address the problem of reducing the clock-rate in MxDFE detectors. Due to the reduced code-rate of 2/3, the channel data-rate is 50% higher than the user data-rate. Hence, for high data-rate applications, it becomes necessary to develop techniques that can achieve reduced clock-rate implementation of the detector. A solution to this was proposed by Kenney and Melas [6]. In their approach, the equalizer is designed to force the first feedback tap to zero. The resulting extra delay of one bit in the feedback path is exploited to develop a detector that employs two critical loops (i.e., comparator, feedback equalizer, and summer) operating on the even and odd samples, respectively. These loops are clocked by clocks that are in exact phase reversal and running at half the channel rate, i.e., only 3/4th of the user rate. This approach, however, requires that the duty cycle of the two clocks be 50%. To this end, we may still have to resort to a master clock at full channel rate and divide that by two. Further, this approach favors analog (continuous-time) front end. If the equalizer is a discrete-time finite impulse response (FIR) filter, it will have to be clocked at full channel rate because it must generate T -spaced samples (T being the channel bit period) for the two critical loops. One approach to overcoming the latter problem is to use two forward equalizers with the taps spaced at $2T$. However, this is not practical because the performance of a $2T$ -spaced equalizer is very poor. Another approach could be to arrange two forward equalizers in a parallel fashion. This, however, would double the complexity of the equalizer.

In this paper, we propose an alternative approach for achieving reduced detector clock-rate. The features of this approach are that 1) the detector needs only one clock running at the user rate; 2) front end equalization can be analog or discrete-time, with the discrete-time front end (if used) also clocked at the user rate; and 3) the detector contains two critical

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Fig. 1. (a) Spectrum of the (1, 7) writing signal and (b) the magnitude responses of the MDFE forward equalizer (two-zeros and four-poles IIR filter), Lorentzian model of recording channel, and a HD channel model, at user density 2.50. The equalizer is designed for the Lorentzian case. The frequencies are normalized by the channel bit-rate. Nyquist frequency = 0.5 Hz. Observe that all spectra are essentially low pass in nature, thereby implying high correlation at the equalizer output.

loops and two FIR interpolation filters—all running at the user rate. Section II presents the principle of the proposed approach. Section III presents the system design. Section IV presents a timing recovery scheme for the proposed reduced-rate detector. Section V presents computer simulation results for MDFE and M2DFE detectors with and without clock-rate reduction. The paper is concluded in Section VI.

II. INTERPOLATION APPROACH FOR CLOCK-RATE REDUCTION

In this section, we first list certain features of (1, 7)-coded channel and MDFE detector that point to the feasibility of reducing the detector clock-rate and then present a block schematic to implement this.

Fig. 1 shows the spectrum of a (1, 7) writing signal and magnitude responses of the recording channel (unequalized Lorentzian model [7] at the user density¹ 2.5) and MDFE forward equalizer. We note the following from this figure. First, most of the energy in the (1, 7) writing signal is concentrated within 25% of the channel bit-rate. Second, the recording channel also has its energy concentrated in the low-frequency region. Third, the MDFE equalizer is essentially low pass in nature. Further, it is well known that the high-frequency energy in the recording channel decreases with an increase in recording density. These features indicate that the signal at the equalizer output should be highly correlated with itself. Therefore, using interpolation, it should be possible to obtain sufficiently accurate estimates of the T -spaced samples from samples taken at larger than T -spacing. This is the key idea behind the clock-rate reduction approach proposed in this paper.

Consider Fig. 2 that shows the discrete-time model of the magnetic recording channel incorporating the MDFE detector running at full channel rate $1/T$. Coefficients of the channel bit response h_k and forward equalizer g_k are at T/L -spacing, where L is the oversampling factor. Input $a(n)$ is the RLL rate $2/3$ (1, 7)-coded data in ± 1 format (i.e., write-current polarity),

¹User density or recording density D_u is defined as $PW50/T_u$, where $PW50$ is the pulsewidth of the channel step-response at 50% amplitude and T_u is the duration of one user bit.

Fig. 2. Discrete-time model of the magnetic recording channel incorporating the MDFE detector (without clock-rate reduction). The taps of channel bit-response h_k and forward equalizer g_k are assumed to be at the fractional spacing of T/L , where T is the channel bit duration and L is the oversampling factor. The cascade of this analog forward equalizer and sampler could be replaced by the cascade of an analog low-pass filter, sampler at rate $1/T$, and a T -spaced FIR forward equalizer, resulting in the so-called digital front end.

b_k 's are the feedback equalizer taps (T -spaced), and $v(m)$ is the channel noise (assumed to be additive white Gaussian). The forward equalizer is assumed to be a discrete-time infinite impulse response (IIR) filter. For practical implementation, this discrete-time IIR equalizer can be transformed into a continuous-time analog equalizer using standard transformations [8, ch. 8]. The approach that we use for designing the IIR equalizer is the procedure given in [7] of first designing a fractionally spaced FIR equalizer with tap-spacing equal to T/L and then designing the IIR equalizer from this FIR equalizer using the equation-error approach. For the sake of ready-reference, Appendix A briefly describes the equalizer design procedure for MDFE that runs at full channel rate.

As mentioned already, our aim is to sample the output of the forward equalizer at a rate that is less than the channel rate $1/T$. Further, we want the critical loop also to work using this reduced rate clock. Because we need to estimate the T -spaced samples from samples taken at the reduced rate, the minimum possible clock/sampling rate will depend on the extent of correlation in the signal. The higher this correlation, the lower the clock-rate can be, and vice-versa. Further, the choice of this reduced clock-rate determines the increase in hardware complexity, i.e., the number of filters required to estimate the T -spaced samples and the configuration of critical loop. For example, if we want the clock-rate to be a fraction x -times

Fig. 3. Block schematic of the MDFE detector with clock-rate reduction. The taps of interpolation filters are at T_1 -spacing. The quantities $z_e(n)$, $z_e(n+1)$, and $z_e(n+2)$ are estimates of the T -spaced samples at instants n , $n+1$, and $n+2$, respectively, and are given by $y(nL + n_0)$, $y(nL + n_0 + L)$, and $y(nL + n_0 + 2L)$, respectively, in terms of the notation used in the text. The sample selector gives $z_e(n)$ to critical loop-1 and $z_e(n+1)$ to critical loop-2 when the $2T_1$ -clock is high, and $z_e(n+2)$ to critical loop-1 when this clock is low. The $2T_1$ -clock is derived from the T_1 -clock by division by 2.

the channel bit rate $1/T$, the number of interpolation filters required will be “ a ,” where a is such that $x = a/b$ with a and b being positive integers that are relatively prime. Hence, we should choose the reduced rate in such a way that the increase in hardware complexity and degradation in performance due to interpolation error are kept within tolerable limits. For this reason, we choose to reduce the clock-rate to user rate (i.e., $x = 2/3$, 33.33% reduction) because this requires only two interpolation filters and a simple critical-loop configuration, as explained below. Nevertheless, the proposed approach can be easily generalized to accommodate clock-rate reduction by any rational fraction.

Fig. 3 shows the block schematic of the MDFE detector with reduced clock-rate equal to user rate $1/T_1$, where $T_1 = 1.5T$. Let us first concentrate on the path labeled “analog front end”; i.e., the forward equalizer is a fractionally spaced (T/L) IIR filter, and sampling is done after equalization. The principle of operation can be explained with the help of the two waveforms shown in Fig. 3. Waveform (a) represents the clock at channel rate $1/T$, and the samples required for detection are shown by $\diamond$ and $*$. The T -clock is used here only for explaining the principle, and it is not used anywhere in the system.² Waveform (b) represents the clock at user rate $1/T_1$ that is used for sampling the equalizer output, and $\diamond$ indicates these T_1 -spaced samples at the equal-

izer output. We assume that the phase of T_1 -clock is such that one in every three T -spaced samples coincide with one of the T_1 -spaced samples, as shown in the figure. Then, the problem we have is to estimate the two T -spaced samples shown by $*$ using the T_1 -spaced samples. Because the relative positions of these two samples are different with respect to the T_1 -spaced samples, we need to use two different interpolation filters for doing this estimation. Clearly, these filters have their taps at T_1 -spacing and are driven by the user-rate clock. Further, observe that we have three T -spaced samples in two periods of the T_1 -clock. Hence, to maintain the detector clock at $1/T_1$, we use two critical loops. As we show below, for this detector configuration to be feasible, it is necessary to provide extra delay in the feedback path. This is done by constraining the first feedback tap to zero.

Fig. 4 shows the arrangement of the two critical loops, giving details of the interconnections. To understand the operation, refer to waveforms (a)–(d). As before, Trace (a) is the clock at channel-rate $1/T$ and is used as a reference. Trace (b) is the actual clock at the reduced-rate $1/T_1$. Traces (c) and (d) are obtained from (b) by division by 2. Because we have three T -spaced samples in two cycles of the T_1 -clock, we cannot have the two critical loops equally share the number of decisions. Therefore, out of the three samples $z_e(n)$, $z_e(n+1)$, and $z_e(n+2)$ that are available during $2T_1$ seconds at the detector input [see Trace (a) in Fig. 3], we arrange the “sample selector” to give $z_e(n)$ to the top loop (i.e., critical loop-1 in

²See Section IV for a timing recovery scheme for deriving the T_1 -clock directly from the analog waveform at the equalizer output.

Fig. 4. Structure of the critical loops shown in Fig. 3 with $T_1 = 1.5T$. (A) When the $2T_1$ -clock is high, both the loops are taking decisions. (B) When the $2T_1$ -clock is low, only the top loop is taking decisions. The feedback taps with solid connections belong to the top loop and those with dashed connections belong to the bottom loop. The number of delay elements and computations required in the bottom loop are only half of that in the top loop. Feasibility of this structure requires the first feedback tap, b_2 , to be zero.

Fig. 3) and $z_e(n+1)$ to the bottom loop (i.e., critical loop-2 in Fig. 3) when the $2T_1$ -clock is high, and $z_e(n+2)$ to the top loop when this clock is low. Thus, the top loop delivers a decision once in every cycle of the T_1 -clock, whereas the bottom loop does this only once in every two cycles. Traces (c) and (d) give the sequences of decisions by the two slicers in these two loops. To make this more clear, Fig. 4(A) shows the connections of the critical loops when the $2T_1$ -clock is high and Fig. 4(B) shows this when the $2T_1$ -clock is low. The feedback taps with “solid” connections belong to the top loop, and those with “dashed” connections belong to the bottom loop. Observe that when this clock is high [Fig. 4(A)], the inputs to taps b_3 ,

b_6 , and b_9 in the top loop come from the shift-register in the bottom loop and that of b_5 and b_8 come from the shift-register in the top loop. On the contrary, these connections are reversed when this clock is low [Fig. 4(B)]. The bottom loop does not need any such extra connections. One advantage of this configuration is that the number of delay elements and computations required in the bottom loop are only half of that in the top loop, thus, saving in complexity and power. Further, it is clear from Fig. 4 that the above configuration would not have been possible if the detector needed the immediate decision $\hat{a}(n-1)$ to make decision on $\hat{a}(n)$. This is ensured by constraining the first feedback tap b_2 to zero during equalizer design. We recall that

this zero-tap condition is also used in the detector configuration proposed in [6].

III. SYSTEM DESIGN

In this section, we give the procedure for designing the forward and feedback equalizers and interpolation filters for MDFE with clock-rate reduction. This procedure is also valid for its advanced versions because the equalizers used in all of these detectors are the same. We first consider the “analog front end” case shown in Fig. 3.

Let $y(n_1L + n_0)$ be the output of the forward equalizer corresponding to the input bit $a(n_1)$. Here, n_0 denotes the delay from channel input to equalizer output. In other words, $y(n_1L + n_0)$ for $n_1 = 1, 2, 3, \dots$, represent the T -spaced samples at the equalizer output. Now, as mentioned in Section II, consider a particular value of “ n ” such that $y(nL + n_0)$ coincide with one of the T_1 -spaced samples at the equalizer output. That is, the samples after downsampling can be represented as $y(nL + n_0 + iP)$ for $P = 1.5L$ and³ $i = 0, \pm 1, \pm 2, \dots$. We need to design the equalizers and interpolation filters for estimating $y(nL + n_0 + L)$ and $y(nL + n_0 + 2L)$ based on $y(nL + n_0 + iP)$, $i = 0, \pm 1, \pm 2, \dots$. Assuming N -tap interpolation filters, these estimates are obtained as

$$\left. \begin{aligned} \tilde{y}(nL + n_0 + jL) &= \sum_{i=1}^N w_{j,i} y(nL + n_0 + (N_1 + j - i)P) \\ &= \mathbf{w}_j^T \mathbf{y}(m_j), \quad j = 1, 2 \\ &= y(nL + n_0), \quad j = 0 \end{aligned} \right\}, \quad (1)$$

where $\mathbf{w}_j = [w_{j,1}, w_{j,2}, \dots, w_{j,N}]^T$ is the j th interpolation filter, $N = N_1 + N_2$ with N_1 (N_2) being the number of T_1 -spaced samples lying to the right (left) of the point of interpolation, $\mathbf{y}(m_j) = [y(m_j - P), y(m_j - 2P), \dots, y(m_j - NP)]^T$, and $m_j = nL + n_0 + (N_1 + j)P$.

The samples used for detection are $\tilde{y}(nL + n_0 + jL)$, and the bits to be detected using these samples are $a(n + j - 1)$, $j = 0, 1, 2$. Clearly, the impulse responses of the three paths resulting in these samples are different because the filters sitting on these paths are distinct from each other. Consequently, the noise and residual intersymbol interference (ISI) at the slicer input for these three samples/phases will be different. Hence, the criterion to be used for designing the forward and feedback equalizers and the interpolation filters should maximize the detection SNR⁴ for each of these three phases. Because the forward and feedback equalizers are common for all three phases, the design of equalizers and interpolation filters should be done in a joint manner rather than separately. As noted in Appendix A, we can also choose to minimize the sum of variances of noise and ISI at the slicer input instead of maximizing the detection SNR.

Let the sum of channel noise and ISI for the three phases be $P_0(\mathbf{g}, \mathbf{b})$, $P_1(\mathbf{g}, \mathbf{b}, \mathbf{w}_1)$, and $P_2(\mathbf{g}, \mathbf{b}, \mathbf{w}_2)$, respectively, where

$\mathbf{g} = [g_0, g_1, \dots, g_{N_f-1}]^T$ is the fractionally spaced FIR forward equalizer tap-weight vector⁵ and $\mathbf{b} = [b_3, \dots, b_{N_b+1}]^T$ is the vector of nonzero feedback taps. The first feedback tap b_2 is constrained to zero, for reasons explained in Section II. Then, using the notation from Appendix A, we have

$$P_j = E \left[(\tilde{y}(nL + n_0 + jL) - \mathbf{b}^T \mathbf{a}(n + j - 1) - a(n + j - 1))^2 \middle| C_j \right], \quad j = 0, 1, 2, \quad (2)$$

where $\mathbf{a}(n) = [a(n - 2), a(n - 3), \dots, a(n - N_b)]^T$ and C_j denotes the condition $a(n + j) \neq a(n + j - 2)$. The second term on the RHS of (2) represents the output of feedback equalizer.

A natural choice for the design criterion, in accordance with the discussion above, should be to minimize the maximum of P_j , $j = 0, 1, 2$. That is

$$\begin{aligned} &\{\mathbf{g}, \mathbf{b}, \mathbf{w}_1, \mathbf{w}_2\} \\ &= \arg \left\{ \min_{\{\mathbf{g}, \mathbf{b}, \mathbf{w}_1, \mathbf{w}_2\}} \left\{ \max_{\{\mathbf{g}, \mathbf{b}, \mathbf{w}_1, \mathbf{w}_2\}} \{P_0, P_1, P_2\} \right\} \right\}. \end{aligned} \quad (3)$$

However, this is a very difficult problem to solve. Hence, the approach that we resort to is to minimize the sum of the three individual cost functions. That is, design $\mathbf{g}$, $\mathbf{b}$, $\mathbf{w}_1$, and $\mathbf{w}_2$ by minimizing

$$\begin{aligned} P_{\text{total}}(\mathbf{g}, \mathbf{w}_1, \mathbf{w}_2, \mathbf{b}) \\ = P_0(\mathbf{g}, \mathbf{b}) + P_1(\mathbf{g}, \mathbf{w}_1, \mathbf{b}) + P_2(\mathbf{g}, \mathbf{w}_2, \mathbf{b}). \end{aligned} \quad (4)$$

Even though it is not immediately clear whether the criteria in (3) and (4) result in the same set of solutions, the simulation results (Section V, Fig. 8) justify the choice of (4). In particular, the degradation in performance due to clock-rate reduction using the solution from (4) turns out to be minimal compared with the case without any reduction. Hence, we believe that the solution obtained by minimizing P_{total} in (4) should be very close to that of (3).

Because the forward equalizer $\mathbf{g}$ appears in series with the interpolation filters $\mathbf{w}_1$ and $\mathbf{w}_2$, the joint minimization of P_{total} with respect to $\mathbf{g}$, $\mathbf{w}_1$, $\mathbf{w}_2$, and $\mathbf{b}$ cannot be done in closed form. Hence, we resort to the following iterative approach.

- 1) *Initialization*: Set the forward equalizer to its optimum, corresponding to the system without reduction in clock-rate (Fig. 2). For this forward equalizer, design the interpolation filters and feedback equalizer by minimizing the cost function P_{total} .
- 2) For the given interpolation filters, design the forward and feedback equalizers by minimizing P_{total} .
- 3) Using the forward equalizer from step 2), design the interpolation filters and feedback equalizer by minimizing P_{total} .
- 4) Repeat steps 2) and 3) until the reduction in P_{total} is not significant.

The design equations required for step 1) are available in Appendix A, and that for steps 2) and 3) are developed in Appendix B.

³Because $P = 1.5L$, the oversampling factor L should be an even number.

⁴See Appendix A for the definition of detection signal-to-noise ratio (SNR).

⁵As mentioned before, the design of the fractionally spaced FIR forward equalizer is an intermediate step for the design of the IIR forward equalizer.

Thus far, all our discussions were limited to the case of analog front end; i.e., the forward equalizer is a continuous-time analog filter, and sampling is done after equalization. The channel output is fed directly to this equalizer. Another front end configuration that is of interest is the case in which the channel output is first fed to an analog low-pass filter for limiting the noise bandwidth, and its output is sampled and fed to a discrete-time FIR forward equalizer. With slight abuse of nomenclature, we use the term “digital front end” to identify this configuration. The interpolation approach proposed above can also be developed for this case. In order to maintain the overall detector clock at the user-rate, the low-pass filter output is sampled at the rate $1/T_1$ and fed to the forward equalizer whose taps are at T_1 -spacing. The equalizer output is then processed using the interpolation filters and critical loops as before (Fig. 3). The design of interpolation filters and equalizers for this system is also outlined in Appendix B.

IV. TIMING RECOVERY FOR REDUCED-RATE DETECTOR

We mentioned in Section II that the proposed detector structure with reduced clock-rate does not need the T -clock for deriving the T_1 -clock ($T_1 = 1.5T$). This means that the timing recovery scheme should be able to do the acquisition and tracking of the T_1 -clock based on the signals sampled at the rate $1/T_1$. In this section, we present a simple scheme that can do this [12]. Our aim is to show that it is possible to directly derive the T_1 -timing from the channel. We assume an analog front end in this section.

In the development of the timing recovery scheme for T_1 -timing, we need to take into account the following points. First, we need to ascertain if the T_1 -spaced samples contain sufficient information for doing reliable timing recovery. Second, 50% of the T_1 -spaced sampling instants do not coincide with the T -spaced instants [see waveforms (a) and (b) in Fig. 3]. As a result, it is not clear how to derive the timing-error signals for these instants because we do not have a convenient target for these samples.⁶ Third, because sampling is done at the input of the interpolation filters and the timing information is derived from their outputs (as we show below), the timing loop has to cope with additional delay due to interpolation filters.

From the discussion in the beginning of Section II, we concluded that the output of the forward equalizer is highly correlated with itself so that the T -spaced samples obtained by interpolation of the T_1 -spaced samples should be reasonably accurate. Further, the interpolation error decreases with an increase in recording density.⁷ Based on this, we can expect satisfactory timing recovery if the density is reasonably high. The second problem of inavailability of timing-error updates at alternative sampling instants can be solved by cleverly manipulating the available timing-error updates. More details on this will be given

in the sequel. The third issue pointed out above, of delay due to interpolation filters, is addressed by explicitly incorporating this delay in the timing recovery scheme developed here. The results show that the performance is satisfactory.

A. Timing Recovery Algorithm and Simulations

The algorithm that we use for deriving the timing information in the $1.5T$ -spaced case is based on the algorithm that is developed for the T -spaced case described in [10]. Let $q(n)$ represent the slicer input for the T -spaced MDFE. The output of the timing error detector (TED) for this system is given by [10]

$$\begin{aligned}\Delta_T(n) &= (q(n) - \hat{a}(n-1))(\hat{a}(n) - \hat{a}(n-2)) \\ &= e_T(n)(\hat{a}(n) - \hat{a}(n-2)),\end{aligned}\quad (5)$$

where $e_T(n) = q(n) - \hat{a}(n-1)$ is the error at the slicer input and $\hat{a}(n-1)$ is the decision at instant n corresponding to the sample $q(n)$. Note from (5) that the TED output is nonzero only when $\hat{a}(n) \neq \hat{a}(n-2)$, i.e., whenever there is a transition in the data-bits. Such samples correspond to inner-eye levels at the slicer input (see Appendix A). Further, because the decision $\hat{a}(n)$ is not available at instant n , the timing error $\Delta_T(n)$, given by (5), will be used at instant $n+1$ instead of n . To develop the TED for the reduced-rate detector, we proceed as below.

We refer to Fig. 5, which depicts the setup we used for doing the timing simulations. For the sake of convenience, we have merged the two critical loops in Fig. 3 into one. The delay due to the interpolation filters has been explicitly accounted for by putting a delay line of duration $4T_1$ (i.e., $6T$) after the sampler. Let n and k denote the indexes corresponding to the T -spaced and T_1 -spaced sampling instants, respectively. Further, let $q_e(n)$ represent the slicer input corresponding to the sample $z_e(n)$, for any n . Then, following (5), we define the timing error for these samples as

$$\begin{aligned}\tilde{\Delta}_T(n) &= (q_e(n) - \hat{a}(n-1))(\hat{a}(n) - \hat{a}(n-2)) \\ &= e_{eT}(n)(\hat{a}(n) - \hat{a}(n-2)),\end{aligned}\quad (6)$$

where $e_{eT}(n) = q_e(n) - \hat{a}(n-1)$. The quantities $q_e(n)$ and $e_{eT}(n)$ are functions of the phase offset τ at the sampler, which is the difference between the ideal and actual sampling instants. Without loss of generality, the ideal sampling instants are assumed to be of the form kT_1 , where k is an integer. Thus, $\tau \neq \tilde{k}T_1$, for a constant integer $\tilde{k}$ implies nonzero phase offset.

Now, assume reference indexes $n = \bar{n}$ and $k = \bar{k}$ such that $z_e(\bar{n}) = y(\bar{n}L + n_0) = y(\bar{k}P + k_0)$, where k_0 is a delay similar to n_0 and $P = 1.5L$ [Note: L is the oversampling factor in the system until the sampler input (see Section III)]. That is, the sampling instant $\bar{k}T_1$ in the T_1 -case coincides with the sampling instant $\bar{n}T$ in the T -case. Because $P = 1.5L$, it is easy to see that

$$\begin{aligned}z_e(\bar{n} + 3l) &= y((\bar{n} + 3l)L + n_0) \\ &= y((\bar{k} + 2l)P + k_0), \quad l = 0, \pm 1, \pm 2, \dots\end{aligned}\quad (7)$$

Thus, the T_1 -spaced instants $\bar{k} + 2l$ coincide with the T -spaced instants $\bar{n} + 3l$ for $l = 0, \pm 1, \pm 2, \dots$. Hence, following (5) and (6), we use $\tilde{\Delta}_T(\bar{n} + 3l)$ to define the timing error for instants $\bar{k} + 2l$. Further, because the T_1 -spaced instants $\bar{k} + 2l + 1$ lie

⁶The difference between the observed signal and its desired value is usually used to derive the timing error information. For example, see [9] and [10].

⁷For example, for the Lorentzian channel given in Fig. 1(b), the magnitude response of the equalized channel (i.e., cascade of channel-bit response and forward equalizer) at the frequency $1/2T_1$, which corresponds to the Nyquist frequency for the user data-rate $1/T_1$, is more than 22 dB below the maximum signal strength in the passband. Further, the total energy beyond the frequency $1/2T_1$ is about 30 dB below the total energy within the band $[0, 1/2T_1]$.

Fig. 6. Transfer characteristics of the TED used for recovering the $1.5T$ -clock for reduced-rate detector (for analog front end) in (a) acquisition mode with the periodic $6T$ pattern as the input, and in (b) tracking mode with random $(1, 7)$ -coded data as the input. The channel used is Lorentzian at user density 2.50. The use of modified threshold shown in Fig. 5 ensures that there are no false-lock phases during acquisition. The linear region of the transfer characteristics during tracking mode is large enough to ensure false-lock free operation [see Fig. 7(b)].

Fig. 7. Phase convergence performance of the timing recovery loop of the reduced-rate detector for recovering the $1.5T$ -clock in (a) noiseless channel with initial phase offset 0.5 and (b) noisy channel with initial phase offset uniformly distributed in $[-0.5, +0.5]$. The phase offset and sampling instants given here are in normalized units (normalization factor = $1.5T$). The channel used is Lorentzian at user density 2.50.

a separate experiment of 100 simulations with the same initial phase $0.5T_1$ and 27 dB SNR, we estimated the root mean square (rms) value of the phase jitter at different time instants during acquisition as well as tracking. Table I shows these values. In this table, the sampling instants are in terms of the reduced-rate clock. So, the end of acquisition corresponds to the 124th instant. Observe that the rms phase jitter at the end of acquisition is less than 1% (normalized to $1.5T$).

V. SIMULATION RESULTS

In this section, we present computer simulation results to demonstrate the performance of MDFE and M2DFE detectors using the proposed clock-rate reduction scheme.

The channel models used in the simulations are the Lorentzian model [7] and a high-density channel model, called the HD model.⁹ The bandwidth of the HD model is narrower than that of Lorentzian [see Fig. 1(b)]. This implies that the correlation in the channel output for the HD model will be

⁹HD model, courtesy of Toshiba Corporation, Japan.

TABLE I
PHASE JITTER PERFORMANCE OF THE TIMING LOOP (LORENTZIAN CHANNEL, USER DENSITY = 2.5, SNR = 27 dB, INITIAL PHASE = $0.75T$, 100 SIMULATIONS)

'analog' front-end		'digital' front-end	
$[N_1 \ N_2]$	SNR(dB) required for BER= $1e-5$	$[N_1 \ N_2]$	SNR(dB) required for BER= $1e-5$
[4 2]	24.77	[3 3]	24.74
[2 4]	25.22	[4 2]	24.67
[3 3]	25.07	[2 4]	24.68
[3 2]	24.93	[3 2]	24.71
[2 3]	25.24	[2 3]	24.73
[4 1]	25.01	[1 4]	24.81
[2 2]	25.23	[2 2]	25.00
		[1 3]	25.39

higher than that for Lorentzian model. Hence, according to the arguments given in the beginning of Section II, for given amounts of recording density and reduced clock-rate, we should expect less performance degradation in the case of HD model compared with Lorentzian. The influence of different

Fig. 8. Performance of MDFE and M2DFE detectors with (dashed line) and without (solid line) clock-rate reduction, using (a) analog front end and Lorentzian channel, (b) analog front end and HD channel, (c) digital front end and Lorentzian channel, and (d) digital front end and HD channel. Analog front end consists of a two-zeros and four-poles IIR equalizer. Digital front end consists of a fourth-order Butterworth low-pass filter with 3 dB cutoff at 40% of the channel Nyquist and a nine-taps FIR equalizer with taps at $1.5T$ -spacing. Feedback equalizer has 12 taps, with the first tap equal to zero. Interpolation is done using two six-tap filters. The 100% MDFE (M2DFE) refers to MDFE (M2DFE) running at full channel rate $1/T$, and the 66.67% MDFE (M2DFE) refers to MDFE (M2DFE) running at user rate $1/1.5T$. The performance degradation due to clock-rate reduction decreases with an increase in density. In M2DFE, the maximum degradation is less than 0.3 dB at 2.25 and about 0.1 dB at 2.75.

heads-media combination on performance is illustrated in our study by using the above two channel models.

The oversampling factor L is set to 4. The number of taps in interpolation filters and feedback equalizer is chosen as 6 ($N = 6$ with $N_1 = 4$, $N_2 = 2$) and 11 ($N_b = 11 + 1 = 12$), respectively. The slicer threshold and buffer length in the M2DFE detector are fixed at 0.20 and 12, respectively. The measure used for illustrating the performance is the SNR [defined in (10)] required to obtain a bit error rate (BER) of 10^{-5} . Over 500 bit errors are used for estimating the error rate at each point of the BER curve.

Fig. 8(a) shows the performance of MDFE and M2DFE detectors with and without clock-rate reduction for a Lorentzian channel using analog front end for user densities 2.25, 2.50, and 2.75. The IIR equalizer has two zeros and four poles and is obtained from a 40-taps T/L -spaced FIR equalizer. Observe that the maximum loss in performance due to clock-rate reduction is less than 0.3 dB. Further, the loss decreases as density increases. This is clearly due to the increased correlation (equivalently, the reduced bandwidth) of the signal at higher densities. Similar curves for the HD channel are shown in Fig. 8(b). Observe that there is some performance gain with clock reduction.

This could be attributed to two factors. First, being a HD channel model, the correlation in the signal is better than that with the Lorentzian model. Hence, the interpolation error will be less. Second, the limited degrees of freedom in the analog equalizer are enhanced by the interpolation filters, leading to better detection SNR.

Fig. 8(c) and (d) show the performance of MDFE and M2DFE detectors using digital front end for Lorentzian and HD channels, respectively. The low-pass filter is a fourth-order Butterworth filter with 3 dB cutoff at 40% of the channel Nyquist. The number of taps in the $1.5T$ -spaced FIR equalizer is 9. Even though the loss is significant for MDFE with Lorentzian, this is not of much concern because we are mainly interested in the performance of advanced versions of MDFE. The maximum loss for M2DFE is still less than 0.3 dB in the Lorentzian case, whereas it is just above 0.1 dB for the HD channel. As before, the degradation in performance due to reduction in clock-rate decreases with an increase in density.

Now, we may remark on the contrasting influence of recording density on equalization and clock-rate reduction. For a given equalizer complexity, it is known that the equalizer performance degrades with an increase in density. On the

TABLE II
PERFORMANCE OF USER-RATE M2DFE DETECTOR FOR DIFFERENT LENGTHS
AND CONFIGURATIONS OF INTERPOLATION FILTERS (LORENTZIAN CHANNEL,
USER DENSITY = 2.5, FILTER LENGTH = $N_1 + N_2$)

‘analog’ front-end		‘digital’ front-end	
$[N_1 \ N_2]$	SNR(dB) required for BER=1e-6	$[N_1 \ N_2]$	SNR(dB) required for BER=1e-6
[4 2]	24.77	[3 3]	24.74
[2 4]	25.22	[4 2]	24.67
[3 3]	25.07	[2 4]	24.68
[3 2]	24.93	[3 2]	24.71
[2 3]	25.24	[2 3]	24.73
[4 1]	25.01	[1 4]	24.81
[2 2]	25.23	[2 2]	25.00
		[1 3]	25.39

other hand, we see from the above results that the relative loss in performance due to reduction in clock-rate decreases with an increase in density. Further, the extra degrees of freedom offered by the interpolation filters could in fact help in minimizing misequalization. Combining these points, we may conclude that the proposed interpolation approach is an efficient means for reducing detector clock-rate in MxDFE detectors, in particular, at high recording densities.

Next, we present some simulation results investigating the effect of interpolation filter length on performance. This study is done for a Lorentzian channel at user density 2.50 using M2DFE detector running at user-rate. Table II shows the SNR required for achieving $1e - 5$ BER for different choices of filter length. The filter length is given by $N_1 + N_2$. Observe that there is not much freedom in the choice of N_1 and N_2 in the analog case. On the other hand, the digital case offers much more flexibility. In this case, even $[N_1 \ N_2] = [1 \ 4]$ appears satisfactory. This is favorable from the point of view of timing recovery because a smaller N_1 means lesser loop delay in the timing loop. This difference between analog and digital cases could be reasoned out as follows. First, there are extra degrees of freedom in the digital case because we are using nine taps for the FIR equalizer. Second, compared with the FIR equalizer, the optimum delay n_0 is much smaller in the IIR equalizer, and the range of values of tolerable n_0 is very narrow.

We also investigated the effect of suboptimal interpolation filters. This study was also done for a Lorentzian channel at user density 2.50 using a M2DFE detector running at user-rate. We replaced the interpolation filters with that obtained by averaging the optimum interpolation filters for user densities 2.25, 2.50, and 2.75. Table III gives these averaged filters. The equalizers were reoptimized, taking into account these fixed interpolation filters. Then, the SNRs required for achieving $1e - 5$ BER at user density 2.50 are 24.77 and 24.75 dB, respectively, for the analog and digital cases. Comparing these numbers with the first column of Table II, we conclude that the interpolation filters can be kept fixed over a reasonably wide range of densities.

VI. CONCLUSIONS

The problem of reducing the detector clock-rate in MxDFE detectors has been addressed, and an interpolation approach has

TABLE III
COEFFICIENTS OF INTERPOLATION FILTERS AVERAGED OVER USER DENSITIES
2.25, 2.50, AND 2.75 (LORENTZIAN CHANNEL)

‘analog’ front-end		‘digital’ front-end	
$[N_1 \ N_2] = [4 \ 2]$		$[N_1 \ N_2] = [3 \ 3]$	
filter-1	filter-2	filter-1	filter-2
-0.0410	-0.0646	0.0480	0.0443
0.1064	0.1235	-0.1454	-0.1153
-0.2412	-0.2427	0.8244	0.4141
0.8844	0.5124	0.4404	0.8424
0.3351	0.7276	-0.1312	-0.1616
-0.0726	-0.0883	0.0661	0.0664
SNR required for 1e-5 BER = 24.77dB		SNR required for 1e-5 BER = 24.75dB	

been proposed. The proposed approach reduces the clock-rate to user data-rate. A timing recovery scheme for recovering the reduced-rate clock has also been developed. Performance simulations using different channel models, recording densities, and front end equalization configurations showed that the degradation in performance due to clock-rate reduction is minimal (less than 0.3 dB SNR), especially for the advanced detectors (M2DFE). To implement this scheme, the detector needs two interpolation filters and two critical loops, clocked using a single clock at user rate. The degradation in performance due to reduction in clock-rate decreases with increase in density. Hence, the current trend of increasing recording density indicates that the proposed approach has potential for wide use in future products.

APPENDIX A

EQUALIZER DESIGN FOR MDFE RUNNING AT CHANNEL-RATE

In this appendix, we briefly recall the procedure given in [7] for designing forward and feedback equalizers for MDFE without any reduction in clock-rate. This is meant to serve as a basic block for designing the system with clock-rate reduction.

Consider the block schematic shown in Fig. 2 incorporating the MDFE detector. Let b_i , $i = 2, 3, \dots, N_b + 1$ be the feedback taps. Because the MDFE system with reduced clock-rate requires the first feedback tap b_2 to be zero (see Section II), we also impose this constraint in the system without clock-rate reduction to ensure that the equalizer structure is the same in both of these systems. The forward and feedback equalizers are designed to achieve a target of the form $f_0 + f_1 D + f_0 D^2$ at the slicer input with $f_1 > f_0 > 0$, where D is the delay operator denoting one-bit delay. This results in a four-level eye at the slicer input (in the absence of noise) because of the $d = 1$ constraint in the RLL (1,7) code; i.e., the ideal slicer input is equal to $f_1 a(n - 1)$ if $a(n) \neq a(n - 2)$ and $(f_1 + 2f_0)a(n - 1)$ if $a(n) = a(n - 2)$. Thus, there is also an inherent detection delay of one bit. Because of this four-level eye, the detection SNR is defined as ratio of the square of the inner-eye level (i.e., f_1^2) to the sum of the variances of noise and residual ISI that is seen at this eye level. The equalizer design can be done by minimizing the sum of this noise and ISI variances, because this is equivalent to maximizing detection SNR. Consequently, the under-

lying mean-squared error cost function is given by (assuming correct decisions)

$$\begin{aligned}
 P(\mathbf{g}, \mathbf{b}) &= E \left[\left(y(nL + n_0) - \sum_{i=3}^{N_b+1} b_i a(n-i) - a(n-1) \right)^2 \right. \\
 &\quad \left. a(n) \neq a(n-2) \right] \\
 &= E \left[\left(\mathbf{g}^T \mathbf{z}(nL + n_0) - \mathbf{b}^T \mathbf{a}(n-1) - a(n-1) \right)^2 \right. \\
 &\quad \left. a(n) \neq a(n-2) \right] \\
 &= \mathbf{g}^T \mathbf{R}_z \mathbf{g} + \mathbf{b}^T \mathbf{R}_a \mathbf{b} - 2\mathbf{g}^T \mathbf{R}_{za} \mathbf{b} - 2\mathbf{g}^T \mathbf{r}_{za} \\
 &\quad + 2\mathbf{b}^T \mathbf{r}_{aa} + 1, \tag{A.1}
 \end{aligned}$$

where

$$\begin{aligned}
 \mathbf{z}(m) &= [z(m), z(m-1), \dots, z(m-N_f+1)]^T, \\
 \mathbf{a}(n-1) &= [a(n-3), a(n-4), \dots, a(n-N_b-1)]^T, \\
 \mathbf{R}_z &= E[\mathbf{z}(nL + n_0) \mathbf{z}^T(nL + n_0) | C_0], \\
 \mathbf{R}_a &= E[\mathbf{a}(n-1) \mathbf{a}^T(n-1) | C_0], \\
 \mathbf{R}_{za} &= E[\mathbf{z}(nL + n_0) \mathbf{a}^T(n-1) | C_0], \\
 \mathbf{r}_{aa} &= E[\mathbf{a}(n-1) a(n-1) | C_0], \\
 \mathbf{r}_{za} &= E[\mathbf{z}(nL + n_0) a(n-1) | C_0],
 \end{aligned}$$

$\mathbf{g} = [g_0, \dots, g_{N_f-1}]^T$ is the fractionally spaced FIR forward equalizer vector, $\mathbf{b} = [b_3, \dots, b_{N_b+1}]^T$ is the feedback equalizer vector, n_0 denotes the delay from channel input to equalizer output, and C_0 refers to the condition $a(n) \neq a(n-2)$. Minimizing $P(\mathbf{g}, \mathbf{b})$ with respect to $\mathbf{g}$ and $\mathbf{b}$, we get the optimum forward and feedback equalizers as

$$\mathbf{g} = [\mathbf{R}_z - \mathbf{R}_{ya} \mathbf{R}_a^{-1} \mathbf{R}_{za}^T]^{-1} [\mathbf{r}_{za} - \mathbf{R}_{za} \mathbf{R}_a^{-1} \mathbf{r}_{aa}], \tag{A.2}$$

$$\mathbf{b} = \mathbf{R}_a^{-1} [\mathbf{R}_{za}^T \mathbf{g} - \mathbf{r}_{aa}]. \tag{A.3}$$

The FIR forward equalizer $\mathbf{g}$ can be converted into an IIR equalizer using the equation-error approach described in [7].

The equalizer design methodology for the case in which the forward equalizer is a T -spaced FIR filter is exactly same as above, except for the following difference. The forward equalizer output $y(nL + n_0)$ is now given by

$$\begin{aligned}
 y(nL + n_0) &= \sum_{i=0}^{N_f-1} g_i z_i((n-i)L + n_0) \\
 &= \mathbf{g}^T \mathbf{z}_l(nL + n_0), \tag{A.4}
 \end{aligned}$$

where g_i 's are coefficients of the T -spaced FIR equalizer and $\mathbf{z}_l(m) = [z_l(m), z_l(m-L), z_l(m-2L), \dots, z_l(m-(N_f-1)L)]^T$. Here, $z_l(m)$ is the sample obtained by passing the channel output $z(m)$ through a low-pass filter meant for limiting the noise bandwidth. So, by replacing $\mathbf{z}(m)$ in the above equations by $\mathbf{z}_l(m)$, we get the optimum T -spaced forward and feedback equalizers.

APPENDIX B

DESIGN EQUATIONS FOR MDFE WITH REDUCED CLOCK-RATE

In this appendix, we derive the expressions for the cost functions P_0, P_1 , and P_2 for the design of equalizers and interpolation filters for the system with reduced clock-rate shown in Fig. 3 [i.e., steps 2) and 3) in the iterative procedure in Section III]. Sections A and B below describe these designs for analog front end and digital front end, respectively.

A. Analog Front End

First, we consider the design of forward equalizer (T/L -spaced FIR filter) $\mathbf{g}$ and feedback equalizer $\mathbf{b}$, assuming given interpolation filters [i.e., step 2)]. The forward equalizer output can be written, in terms of the input $z(m)$, as

$$\begin{aligned}
 y(m) &= \sum_{i=0}^{N_f-1} g_i z(m-i) = \mathbf{g}^T \mathbf{z}(m), \\
 \mathbf{z}(m) &= [z(m), z(m-1), \dots, z(m-N_f+1)]^T. \tag{B.1}
 \end{aligned}$$

Substituting (B.1) in (1) and doing some manipulations, we get

$$\begin{aligned}
 \tilde{y}(nL + n_0 + jL) &= \mathbf{w}_j^T \mathbf{y}(m_j) \\
 &= \check{\mathbf{y}}_j^T(m_j) \mathbf{g}, \quad j = 1, 2, \tag{B.2}
 \end{aligned}$$

where $\check{\mathbf{y}}_j(m_j) = [\check{y}_j(m_j - P), \check{y}_j(m_j - P - 1), \dots, \check{y}_j(m_j - P - N_f + 1)]^T$ and $\check{y}_j(m) = \sum_{i=0}^{N_f-1} w_{j,i} z(m_j - iP)$, $j = 1, 2$. Substituting (B.1) and (B.2) in (2), we get the individual cost functions P_j as

$$\begin{aligned}
 P_j(\mathbf{g}, \mathbf{b}) &= E \left[\left(\mathbf{g}^T \mathbf{z}(nL + n_0) - \mathbf{b}^T \mathbf{a}(n-1) \right. \right. \\
 &\quad \left. \left. - a(n-1) \right)^2 \middle| C_0 \right], \quad j = 0, \tag{B.3}
 \end{aligned}$$

$$\begin{aligned}
 &= E \left[\left(\mathbf{g}^T \check{\mathbf{y}}_j(m_j) - \mathbf{b}^T \mathbf{a}(n+j-1) \right. \right. \\
 &\quad \left. \left. - a(n+j-1) \right)^2 \middle| C_j \right], \quad j = 1, 2. \tag{B.4}
 \end{aligned}$$

The overall cost function $P_{\text{total}}(\mathbf{g}, \mathbf{b})$ given by $P_0(\mathbf{g}, \mathbf{b}) + P_1(\mathbf{g}, \mathbf{b}) + P_2(\mathbf{g}, \mathbf{b})$ is quadratic in $\mathbf{g}$ and $\mathbf{b}$. Hence, it is straightforward to solve for the optimum $\mathbf{g}$ and $\mathbf{b}$. The FIR equalizer $\mathbf{g}$ is then converted to the IIR form as in [7].

Next, we consider the design of interpolation filters and feedback equalizer, assuming a given forward equalizer (IIR filter) [i.e., step 3)]. Substituting (1) into (2), we get the expressions for the individual cost functions as

$$\begin{aligned}
 P_j(\mathbf{w}_j, \mathbf{b}) &= E \left[\left(\mathbf{w}_j^T \mathbf{y}(m_j) - \mathbf{b}^T \mathbf{a}(n+j-1) \right. \right. \\
 &\quad \left. \left. - a(n+j-1) \right)^2 \middle| C_j \right], \quad j = 1, 2, \tag{B.5}
 \end{aligned}$$

$$\begin{aligned}
 &= E \left[\left(y(nL + n_0) - \mathbf{b}^T \mathbf{a}(n-1) \right. \right. \\
 &\quad \left. \left. - a(n-1) \right)^2 \middle| C_0 \right], \quad j = 0. \tag{B.6}
 \end{aligned}$$

Clearly, the overall cost function $P_{\text{total}}(\mathbf{w}_1, \mathbf{w}_2, \mathbf{b})$ given by $P_0(\mathbf{b}) + P_1(\mathbf{w}_1, \mathbf{b}) + P_2(\mathbf{w}_2, \mathbf{b})$ is quadratic in $\mathbf{w}_1, \mathbf{w}_2$, and $\mathbf{b}$. Hence, it is straightforward to solve for the optimum interpolation filters $\mathbf{w}_1$ and $\mathbf{w}_2$ and feedback equalizer $\mathbf{b}$.

Now, if we closely examine the task accomplished by the interpolation filters, we will see that they are like phase-shifters, in a broad sense. If the channel characteristics do not change significantly from some nominal specifications, the characteristics of these phase-shifters also will not change much. We may exploit this to simplify practical implementation by freezing the coefficients of the interpolation filters. However, we may redesign the forward and feedback equalizers to minimize the degradation in performance due to misequalization. Further, if there is some mismatch between the resulting FIR and IIR forward equalizers, the feedback equalizer will not be optimum when used along with the IIR equalizer. Hence, we need to re-optimize the feedback equalizer to account for this mismatch. This is done by minimizing the sum of the mean-squared values of ISI at the slicer input for the three phases, assuming known interpolation filters and the IIR forward equalizer. Consider the cost functions $P_j(\mathbf{w}_j, \mathbf{b})$ given in (B.5) and (B.6). If the interpolation filters are assumed to be fixed, these functions represent the mean-square value of the ISI at the slicer input as a function of the feedback taps, along with a fixed amount of noise variance. Hence, it is straightforward to solve for the optimum feedback equalizer $\mathbf{b}$ for the given interpolation filters and the IIR forward equalizer.

B. Digital Front End

For a given forward equalizer ($1.5T$ -spaced FIR equalizer), the cost functions required for the design of interpolation filters and feedback equalizer are the same as those given by (B.5) and (B.6).

The cost functions required for the design of a forward equalizer ($1.5T$ -spaced FIR filter) and a feedback equalizer, assuming given interpolation filters [i.e., step 2)], are similar to those in (B.3) and (B.4), except for the following two differences. First, the vector $\mathbf{z}(nL + n_0)$ in (B.3) should be replaced by

$$\tilde{\mathbf{z}}_l(nL + n_0) = [z_l(nL + n_0), z_l(nL + n_0 - P), \dots, z_l(nL + n_0 - (N_f - 1)P)]^T,$$

where $z_l(m)$ is the output of the low-pass filter. Second, the vector $\tilde{\mathbf{y}}_j(m_j)$ in (B.4) should be redefined as

$$\tilde{\mathbf{y}}_j(m_j) = [\tilde{y}_j(m_j - P), \tilde{y}_j(m_j - 2P), \dots, \tilde{y}_j(m_j - N_f P)]^T,$$

where $\tilde{y}_j(m) = \sum_{i=0}^{N-1} w_{j,i} z_l(m_j - iP)$ for $j = 1, 2$.

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