DFE Timing Acquisition: Analysis and a New Approach for Fast Acquisition

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Abstract—The problem of timing acquisition in decision feedback equalization (DFE) detectors for magnetic recording channels, in particular the multi-level DFE (MDFE), is considered. We first address the issue of the optimal choice of preamble pattern for timing acquisition and show that a 6T periodic pattern (T being the bit period) is optimum for medium to high user densities. Next, we show that the MDFE timing-error detector using the 6T-pattern is near optimum for acquisition. Finally, we propose a novel threshold-based fast acquisition scheme that can eliminate false lock and effectively prevent hang up problems.

Index Terms—Timing acquisition, preamble pattern, TED, false lock, hang up, magnetic recording, DFE, MDFE.

I. INTRODUCTION

AST and accurate acquisition of clock timing is an essential prerequisite for reliable data detection in magnetic recording. Normally, a periodic clock run-in pattern, called preamble, is used for providing timing information during acquisition. The speed and accuracy of timing acquisition are determined mainly by the effective timing SNR (signal to noise ratio) of the preamble signal and the timing-error detector (TED) used in the timing recovery loop. The TED performance can be assessed by computing the loss in TED efficiency compared to that of the optimum maximum-likelihood (ML) TED [1], [2]. Using these measures, we examine the optimality of preamble pattern and TED used in MDFE.

False lock and hang up are two serious problems that arise during timing acquisition. Timing acquisition can be hindered completely by false lock in the timing loop, and its speed can be retarded significantly by hang up. In DFE timing acquisition, these problems become more serious because of wrong decisions in the feedback filter due to possibly large initial timing, gain, or DC errors. In [3], the use of special equalizer coefficients and switches are proposed to overcome false lock and hang up in MDFE TED. In this paper, we propose a novel technique using a modified threshold scheme to solve these problems. It also has a more general form and can tolerate large initial errors in gain and DC-offset.

In Section II, we investigate the optimal choice of preamble pattern. In Section III, we show that the MDFE TED with the 6T pattern (+++ - - -) is near optimum. In Section IV, we propose a modified threshold-based fast timing acquisition scheme for DFE-type detectors, and present simulations for MDFE channel. The paper is concluded in Section V.

II. OPTIMALITY OF PREAMBLE PATTERN

The optimality of preamble pattern can be assessed using the effective timing SNR of the replay signal at the recording channel output (i.e., input of forward equalizer in Fig. 2). The effective timing SNR is defined as the ratio of the average power in the time derivative of the signal to noise variance. For a periodic preamble pattern, the replay signal is essentially sinusoidal, say, at frequency \( f_0 \). Neglecting the harmonics and normalizing the variance of channel noise (additive white Gaussian) to 1, we can compute the effective timing SNR of the replay signal as

\[
\text{SNR}' = [2\pi f_0 \cdot H(f_0)]^2
\]

where \( H(f) \) is the channel frequency response and \( f \) is the frequency variable normalized by the bit-rate 1/T. For the Lorentzian channel model with user density \( D_u \), \( H(f) \) is

\[
H(f) = \pi T \cdot (D_u/R_{\text{code}}) \cdot (\pi f)^2 c^{-\pi D_u M/\pi R_{\text{code}}}
\]

where \( R_{\text{code}} \) is the code rate of the channel encoder.

We consider the use of 4T, 6T and 8T preamble patterns, which result in single-frequencies at 1/4T, 1/6T and 1/8T, respectively, and compute the timing SNR of the replay signal for various user densities. The results are shown in Fig. 1 for the rate 2/3 (1,7) coded Lorentzian channel. This is the code used
in MDFE, which is the subject of the next two sections. Observe that the $4T$-pattern is optimal for very low densities and the $8T$-pattern for very high densities. Thus, the $6T$-pattern preamble is the preferred pattern for medium to high densities.

Computing the timing SNR at the equalizer output results in similar conclusions as above. In fact, these conclusions could also have been reached by investigating the efficiency of maximum likelihood timing recovery for each of the above preamble patterns [1].

III. OPTIMALITY OF MDFE TED

Having chosen a suitable preamble pattern, the acquisition performance depends heavily on the type of TED scheme used [2]. We consider the MDFE detection scheme used in (1,7) coded channels [4], [5] and analyze its TED performance during acquisition. MDFE detector has a simple structure and offers relatively good performance for medium to high densities [5], [6]. The output of the transition based TED used in MDFE [3] is given by

$$\Delta(t) = (\hat{a}_k(t) - \hat{a}_k) \cdot (\hat{a}_{k+1} - \hat{a}_{k-1})$$

(3)

where $\hat{a}_k(t)$ is the slicer input at time instant $kT + \tau$, $\tau$ is timing offset, and $\hat{a}_k$ is the corresponding decision at the slicer output. We assess the TED performance by comparing its efficiency with that of the ML TED [1], [2]. TED efficiency is a measure of its ability to extract timing information while rejecting noise. Following [1], TED efficiency is defined as

$$\gamma = \frac{1}{\text{SNR}} \cdot \frac{K}{\sigma^2}$$

(4)

where $\text{SNR} = \int_{-\infty}^{\infty} |H(f)|^2 \, df / N_0$, $N_0$ is the power spectral density of the channel noise (white), $K$ is the slope of the TED transfer function (timing function) at origin, and $\sigma^2$ is the variance of phase noise at TED output.

Using (4) and (3), the efficiencies of ML and the MDFE TED’s can be obtained as

$$\gamma_{\text{ML}} = \left| 2\pi f_0 H(f_0) \right|^2 \int |H(f)|^2 \, df$$

(5)

$$\gamma_{\text{MDFE}} = \left| 2\pi f_0 \text{Re}[Q(f_0)] \right|^2 W(f_0) \int |H(f)|^2 \, df$$

(6)

where $Q(f)$ and $W(f)$ are frequency responses of the MDFE equalized channel and the forward equalizer, respectively, and $Q(f) = H(f)W(f)$. We define the efficiency loss of MDFE TED as the ratio $\gamma_{\text{ML}} / \gamma_{\text{MDFE}}$. Table I gives this loss over a range of user densities based on the $6T$ preamble pattern for Lorentzian channel. A loss factor of 2 means that the timing-jitter variance at TED output will be twice as large for the same channel and timing loop parameters. Observe that the loss of MDFE TED is small even at very high densities. This suggests that the transition-based MDFE TED is near optimum for timing acquisition.

IV. MODIFIED THRESHOLD-BASED FAST ACQUISITION

It was shown in [3] that the MDFE TED given by (3) suffers from false lock and hang up problems. Instead of using the special equalizer coefficients and two switches to overcome these problems [3], we propose a novel technique that is simpler and more general. The simulations reported here are for the Lorentzian channel at user density 3.0, with a 2-zero 4-pole forward equalizer and a 10-tap feedback equalizer.

The proposed scheme is depicted in Fig. 2. The modified threshold filter has output

$$c_k = \lambda_1 \cdot (\hat{a}_{k-3} - \hat{a}_{k-3}) + \lambda_2 \sum_{i=1}^{6} \hat{a}_{k-3}$$

(7)

where $\lambda_1$ and $\lambda_2$ are two real-valued scale-factors. Typically, $\lambda_1 = 1$ and $\lambda_2 = 1/6$ for the $6T$ preamble pattern. The main idea is to modify the slicer threshold appropriately to ensure that the $6T$-pattern with correct phase is recovered at the slicer output to avoid false lock, and to introduce hysteresis into the timing loop to prevent hang up.

A similar idea was earlier proposed in [7] for timing acquisition in partial response channels using $4T$-pattern preamble. The modified threshold used in [7] is $c_k = \lambda_1 \cdot \hat{a}_{k-2}$. This introduces hysteresis effect for preventing hang up. However, this cannot be used directly in DFE since wrong decision feedback due to initial errors in phase, gain or DC can easily lead to false lock. To illustrate this, we did the following. With a fixed DC-offset of 0.5 at the slicer input, we estimated the timing function using $6T$-pattern in the presence of the modified threshold $c_k = \hat{a}_{k-3}$. Doing this for all possible initial conditions in the feedback register and for timing offsets ranging from $-3$ to $3$, and plotting the results together, we get the timing function shown in Fig. 3(a).

Observe that even though hysteresis effect has been introduced, there are some false-lock spots on incorrect phases around $\pm 0.5$. This is further illustrated in Fig. 3(b) that shows the phase-convergence curves with closed timing loop for the
initial phase 0.5. There would be no false lock if DC-offset is zero. Careful examination revealed that the false lock phases correspond to decision patterns different from the desired 6T-pattern “+++ −−−”. Further studies showed that for certain initial offset in DC and phase, false lock could happen even with closed DC and timing loops. Thus, we may conclude that the simple threshold $c_k = \hat{a}_{k-3}$ fails to prevent false lock in the presence of significant DC errors. However, false lock was not observed when the noise level in the channel was high. We also made similar investigation on the effect of fixed gain error at the slicer input. We observed several false lock phases when the slicer input gain was set to 0.5 (ideal gain being 1.0). Note that studying the effect of gain at the slicer input is analogous to gain studies in nonfeedback systems such as partial response channels.

Now, we will show that the modified threshold scheme given by (7) can effectively solve this false lock problem while maintaining the hysteresis effect. This threshold helps to convert any wrong pattern in the feedback register into the 6T-pattern with correct phase. The first term, $\lambda_1 (\hat{a}_{k-3} - \hat{a}_{k-5})$, in (7) forces the slicer output sequence to obey $\hat{a}_k = -\hat{a}_{k-3}$, which any 6T-pattern should satisfy. The second term forces the slicer output to have zero DC over any block of 6 bits, since any 6T-pattern should satisfy this too. For a valid 6T-pattern of any phase, the modified threshold $c_k$ is in the form “... −2 −2 0 +2 +2 0 +2 −2 0 +2 +2 0 ...”. Using this sequence, the slicer makes a decision $\hat{a}_k$ to be +1 (resp. −1) when $c_k$ is −2 (resp. +2), and to be +1 or −1 when $c_k$ is zero. This successfully builds in hysteresis effect and equips the slicer with the ability to shift a 6T-pattern with wrong phase to that with correct phase. In conclusion, by using the proposed modified threshold (7), the slicer can convert any wrong pattern in the feedback register into the 6T “+++ −−−” pattern with correct phase.

Using the proposed threshold scheme, we repeated the simulations of Fig. 3, and the results are shown in Fig. 4. Observe that there are no false-lock phases. Further, the hysteresis range is significant. Hence, hang-up problem arising from large phase jitter is less probable. This scheme does not result in false lock even when there is a fixed gain of 0.5 at the slicer input, while retaining the hysteresis effect. Detailed studies showed that this scheme can tolerate gain at the slicer input from 0.5 to 2.0, and DC-offset from −0.5 to +0.5. The oscillatory nature that is observed in the phase convergence curves of Figs. 3(b) and 4(b) is because of the presence of fixed DC-offset. These curves would have been smooth if the DC-offset was zero or if the DC loop was closed.

To thoroughly study the performance of MDFE TED with the proposed modified threshold scheme, we performed Monte-Carlo simulations using a second-order phase-locked loop. Initial phase and frequency errors were 50% and 0.1% of the clock-cycle, respectively. Initial gain was set to 0.5 and DC-offset to 0.35. The channel SNR, which is defined as the ratio of base to peak of isolated transition response to RMS noise in user bandwidth, is 23 dB. We conducted 5000 simulations at user density 3.0, with closed timing-phase, frequency, DC and gain loops. The resulting phase convergence curves are plotted in Fig. 5. The length of 6T-pattern preamble is 192 bits. The modified threshold scheme is disabled after the acquisition phase. At time instant 180, which is close to the end of acquisition phase, the RMS value of jitter in the phase is estimated to be less than 1.8%. Close examination revealed that the contents of feedback register converge from any initial random pattern to the correct 6T-pattern within about 25 bits.

Finally, the modified threshold scheme proposed above can be generalized to provide a threshold sequence

$$c_k = \lambda_1 \cdot (\hat{a}_{k-M/2} - \hat{a}_{k-M+1}) + \lambda_2 \cdot \sum_{i=1}^{M} \hat{a}_{k-i}$$  \hspace{1cm} (8)

that can be used with preamble patterns having period $M$ bits, for even $M$. Typically, $\lambda_1 = 1$ and $\lambda_2 = 1/M$. 

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**Fig. 3.** Study of MDFE TED with modified threshold $c_k = \hat{a}_{k-3}$ and a fixed DC-offset 0.5 at the slicer input, for noiseless channel.

**Fig. 4.** Study of MDFE TED with the proposed modified threshold (7) and a fixed DC-offset 0.5 at the slicer input, for noiseless channel.

**Fig. 5.** Sampling phase acquisition and tracking for MDFE TED at user density 3.0 and 23 dB SNR.
V. CONCLUSION

We examined the problem of fast timing acquisition for DFE detectors. The $6T$-pattern preamble has been shown to provide the best timing SNR for medium to high recording densities, on rate 2/3 (1,7) Lorentzian channels. With this preamble, the transition-based timing-error detector used in MDFE has been shown to be near optimum during acquisition. Finally, a modified threshold scheme has been proposed to overcome the problems of false lock and hang up, thus providing a novel and simple fast acquisition scheme. Simulations showed that this scheme can tolerate large initial errors in gain and DC-offsets.

REFERENCES


