A Digital Implementation of a Frequency Steered Phase Locked Loop

Martin T. Hill, Student Member, IEEE and Antonio Cantoni, Fellow, IEEE

Abstract—A digital implementation of a new technique that delivers an extremely accurate and stable phase locked loop system (PLL) is presented. The new technique uses competing phase and frequency loops to incorporate an accurate local reference frequency into the phase locked loop structure. Disturbances on the phase loop caused by the digital frequency loop are identified and a method to mitigate the disturbances is developed. The implementation is primarily designed for high-speed clock and data recovery and experimental results from a clock recovery system for nonreturn to zero data streams at 155.52 MHz are presented.

Index Terms—Clock-recovery, digital, frequency-locked loop, phase-locked loop, phase-noise.

I. INTRODUCTION

The integration on silicon of clock and data recovery circuits has received considerable attention in the literature. This paper presents an implementation of a new technique that effectively delivers a very accurate and stable phase locked loop (PLL) system. The implementation is primarily designed for high-speed clock and data recovery. However, due to the high stability and well understood mathematical model the new technique provides, it can be used for other demanding applications.

It is common for voltage controlled oscillators (VCO’s) implemented in integrated circuit technology to have very poorly specified center frequencies and high gain, making their use for low bandwidth applications such as clock recovery difficult. The issues that have been addressed by previous clock recovery circuits include reliable locking by accurate centering of the VCO in the PLL. Avoidance of sideband locking and accurate free run frequency when no input signal is present. Some of these issues have been solved using the following techniques:

• Reliable locking has been achieved by employing frequency detectors in addition to a phase detector [1]. This technique is generally used where the VCO center frequency is reasonably close to the data rate and does not address the issue of accurate free run frequency.
• High-speed digital PLL’s using novel methods to generate the very high-speed clocks and to process the phase information have been employed in low and medium rate clock recovery circuits [2].
• A master/slave dual loop architecture employing highly matched VCO’s has been used to help center the VCO [3].

Transmission data rates are specified with tolerances in the order of several parts per million (ppm) [6] in modern communication systems. A new technique called the steered frequency phase locked loop (SFPLL) (patent pending) is presented in [7]. The new technique allows the PLL used for clock recovery to be centered at the appropriate frequency, with the same accuracy associated with the transmitter, independent of the quality of its VCO.

This paper is organized as follows. In the rest of this section the basic structure of the SFPLL is described. In Section II an overview of the implementation is given. Then in Section III and Section IV the phase and frequency loops of the SFPLL are examined. In Section V and Section VI a method to mitigate the disturbances of the frequency loop on the phase loop is described. Finally experimental results for a clock recovery system operating at 155.52 MHz are given.

The structure of the SFPLL is shown in Fig. 1. In Fig. 1 the gains of the components are: phase detector $K_{pd}$, frequency detector $K_{f}$, and VCO $K_{o}$. $K_{p}$ and $K_{f}$ is additional gain. $F_{f}(s)$ is a filter which does not have poles at the origin. $F_{c}(s)$ is a filter which has one pole at the origin.

The SFPLL can be thought of as two parts in competition against each other: a phase loop and a frequency loop. The frequency loop acts to force the VCO to be equal to the reference frequency $\omega_r$. The reference frequency $\omega_r$ is chosen to be close to (though not necessarily the same as) the frequency of the input signal which the SFPLL is required to lock to. The phase loop acts to force the VCO to be equal to the frequency of the input signal. For a controllable range of input signal frequencies the phase loop is able to lock to the input signal. The phase loop uses a static phase error to counteract the effects of the frequency loop. A complete mathematical description is given in [7], however, key results obtained from a simple linear analysis of the SFPLL are as follows.

• When no input signal is present the output frequency is $\omega_r$.
• When the phase loop locks to a signal of frequency $\omega$ there will be a static phase error $\theta_e$ between the SFPLL output and input signal

\[ \theta_e = \frac{K_{pd}K_{f}}{K_{pd}K_{p}} (\omega - \omega_r). \] (1)
II. SYSTEM OVERVIEW

The digital implementation of the SFPLL is shown in Fig. 2. The components in the implementation Fig. 2 correspond to the blocks in the model Fig. 1 as follows.

The phase detector, frequency detector, and VCO are the same in both model and implementation. The digital filter in the implementation corresponds to the filter $F_f(s)$. The digital combiner corresponds to the summer in the model.

The resistor and capacitor correspond to the filter $F_c(s)$ in the model. $F_c(s)$ has a pole very close to the origin and a zero. The output from the digital combiner is a current. This current source is achieved with a charge pump on the output of the digital combiner. Standard PLL's employing charge-pumps [1], [9] realize a filter with a pole close to the origin in the same way. $F_c(s)$ does not have a pole exactly at the origin (i.e., perfect integrator) due to leakage currents in the charge pump, capacitor, and VCO input. Typically, these leakage currents are very small, resulting in $F_c(s)$ with a pole very close to the origin and the SFPLL being centered within several ppm of the reference frequency.

The additional gains $K_p$ and $K_f$ in the model are related to the magnitude of the digital combiner charge pump current.

The parameters of the system and how they relate to system performance requirements are now given.

- The small-signal linear behavior of the phase loop only of the SFPLL is completely specified by the damping factor $\zeta_p$ and the natural frequency $\omega_n$ [8]. The approximate open loop crossover frequency $\omega_c$ and $\zeta_p$ can be derived from system performance requirements parameters. For example, jitter transfer mask in [6] will result in an upper bound for $\omega_c$ and a lower bound on $\zeta_p$.
- The steady-state phase error $\theta_e$ (1) under worst case frequency offsets, i.e., maximum $\omega - \omega_r$.
- The frequency loop of the SFPLL must be stable and, hence, have a sufficiently high damping factor $\zeta_f$.
- The reference frequency is normally a submultiple, $(f_r/m)$ of the SFPLL output frequency $f_o$.
The maximum clock rate at which the various digital components can be run at will typically be a submultiple of the SFPLL output frequency $f_c$.

An important parameter $\lambda$, which will be used extensively, is defined by

$$\lambda = \frac{K_{pd}K_f}{K_{pf}K_p}.$$  

### A. Phase and Frequency Detectors

Phase detectors can be constructed using digital logic gates and/or flip flops and the individual designs and characteristics are covered extensively in the literature, e.g., [10]. Note that the phase detectors considered do not have additional frequency detection characteristics.

A typical phase detector characteristic is periodic, with a period normally of $2\pi$. Near zero phase difference the phase detector can be approximated with a linear characteristic of gain parameter $K_{pf}$. The periodic phase detector characteristic will have a maximum value, denoted here as $PD_{\text{max}}$. The maximum phase error $\theta_{\text{max}}$ is defined as

$$\theta_{\text{max}} = PD_{\text{max}}/K_{pf}. \quad (2)$$

The phase detector parameters of relevance to the rest of this paper are $K_{pf}$ and $\theta_{\text{max}}$.

The frequency detector considered in this paper is described by Messerschmitt in [11] and is called the rotational frequency detector. It is implemented using purely digital components such as flip flops and logic gates. The rotational frequency detector outputs a pulse every time the reference clock ($\omega_r$) phase slips past the VCO clock ($\omega_c$). The rate at which the detector outputs pulses indicates the magnitude of the frequency difference $\omega_r - \omega_c$. The gain of the rotational frequency detector $K_{fd}$ is

$$K_{fd} = 1/\omega_r. \quad (3)$$

### III. PHASE LOOP PARAMETERS

Based on the results presented in [8], the values of the filter components $R$ and $C$ can be found in terms of $\omega_c$, $\zeta_p$, $K_{pf}$, and $K_{pd}$

$$R = \frac{\omega_c}{K_{pd}K_cI_p} \quad (5)$$

$$C = \frac{4\zeta_p^2K_{pd}K_cI_p}{\omega_c^2}. \quad (6)$$

Consider for the moment that the digital combiner (Fig. 2) is removed and that the phase and frequency detectors each have a charge pump. The outputs of the two charge pumps are tied together and pump current into the $RC$ filter. The digital combiner will be introduced and a charge pump eliminated in Section V.

$I_p$ is the phase detector charge pump current, and is defined as the additional gain factor $K_p$. The frequency detector charge pump current $I_{fd}$, defined as the additional gain factor $K_{fd}$, can be found

$$I_{fd} = \frac{\lambda K_{pd}K_f}{K_fK_c}. \quad (7)$$

When the frequency detector pumps current into the $C$ it causes phase and frequency disturbances to the phase loop. If these disturbances are too great they will cause the phase loop to lose lock. There are two disturbance mechanisms.

The first disturbance is a phase disturbance $\theta_d$. It is caused when the frequency detector pumps current through $R$, thus causing a short term shift in the VCO voltage and, hence, a phase jump. For the phase loop to maintain lock $\theta_d$ must be less than $2\pi$. In fact, for reliable operation and low phase jitter on the SFPLL output condition (8) must be met.

$$\theta_d < 2\pi. \quad (8)$$

If the current pulse from the frequency detector lasts for one VCO clock period, i.e., $2\pi/\omega_c$, then from (5) and (7) and applying the condition of (8), the following relating phase disturbance as a fraction of one cycle (i.e., $2\pi$) is obtained:

$$\frac{\theta_d}{2\pi} = \frac{\lambda}{K_fK_c\omega_c} \ll 1. \quad (9)$$

The second disturbance is a frequency disturbance $\omega_d$. It is caused by the voltage on $C$ being shifted as a result of current being pumped into $C$. Hence, the VCO has a shifted voltage applied to it. The phase loop will eventually counteract this through its phase error, $\theta_d$, providing the phase loop remains locked. For the phase loop to maintain lock $\omega_d$ must be less than the pull-out frequency of the phase loop [12] which is for a highly damped type II PLL approximately $\omega_c$. For reliable operation and low jitter on the SFPLL output the condition (10) must be met

$$\omega_d < \omega_c. \quad (10)$$

If the current pulse from the frequency detector lasts for one VCO clock period, then from (6) and (7) and applying the condition of (10), the following relating $\omega_d$ as a fraction of $\omega_c$ is obtained:

$$\frac{\omega_d}{\omega_c} = \frac{\pi \lambda}{2K_{pd}K_c\omega_c} \ll 1. \quad (11)$$

Now consider the situation where the reference clock input is not $\omega_r$ but instead is a submultiple $\omega'_m$, i.e.,

$$\omega'_m = \frac{\omega_r}{m}. \quad (12)$$

where $m$ is an integer.

This situation is likely to be the norm as first, the frequency detector actually needs to be run at the rate $4\omega'_m$ (see [11]) and second, the range of frequencies at which low cost crystal oscillators (which will most likely provide $\omega'_m$) operate is limited to a few tens of megahertz. To perform a valid comparison with $\omega'_m$, $\omega_c$ also has to be similarly scaled down and the rate at which phase slips of one cycle between $\omega'_m$ and $\omega''_m$ occur is also reduced by $m$. 

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The slip rate is also the rate at which the frequency detector emits pulses and the gain of the frequency detector is reduced by a factor of \(m\). To maintain the same frequency loop gain the duration of the frequency detector current pulse must be increased \(m\) times or the current \(I_{ff}\) increased \(m\) times. Either way, the disturbance to the phase loop is increased \(m\) times, even though it will occur \(m\) times less often.

### IV. Frequency Loop Parameters

Consider for the moment that the resistor \(R\) in the loop filter is replaced by a short circuit. The open loop transfer function of the frequency loop is

\[
\frac{K_H}{s}.
\]

\(K_H\) is related to other system parameters

\[
K_H = K_{fd} I_{ff} \frac{1}{C} K_0 = \frac{\lambda \omega_c}{4k_p^2}.
\]  

If a pole at frequency \(\omega_p\) is introduced by the digital filter, the frequency loop becomes a second-order system. The positioning of the pole \(\omega_p\) will affect the closed loop stability and damping factor \(\zeta_f\). A general requirement is that the frequency loop is stable and, hence, the damping is sufficient. \(\omega_p\) can be determined in terms of \(\zeta_f\) and other system parameters

\[
\omega_p = \frac{\lambda \omega_c^2 \zeta_f^2}{\zeta_p^2}.
\]

Considering now the effect of the \(R\) on the frequency loop, the effect of \(R\) is to introduce a zero at frequency \(\omega_z\) in the frequency loop, which enhances frequency loop stability.

### V. Disturbance Reduction

One method of reducing the sudden phase and frequency disturbance of each pulse from the frequency detector discussed in Section III, is to spread the pulse out over a long period of time. This can be done by breaking the pulse up into a large number of smaller pulses, as shown in Fig. 3. Each frequency detector pulse is broken up into \(N_s\) smaller pulses, each of \(N_{vp}\) VCO clock periods wide, and spaced at \(N_{vp}N_s\) VCO clock periods. Thus \(I_{ff}\) is reduced, effectively decoupling it from \(K_f\). The new frequency loop output current \(I_f\) is defined as

\[
I_f = I_{ff} m \frac{N_{vp} N_s}{N_{vp} N_s},
\]

The new phase and frequency disturbances for each of the smaller pulses of width \(N_{vp}\) are reduced from (9) and (11) by a factor \(N_s\)

\[
\frac{\theta_d}{2\pi} = \frac{m\lambda}{N_s K_{fd} \omega_c} \ll 1
\]  

\[
\frac{\omega_d}{\omega_c} = \frac{m\pi \lambda}{2N_s K_{fd} K_p^2 \omega_c} \ll 1.
\]

Having \(I_f\) now decoupled from \(K_f\) provides freedom in choosing \(I_f\). The frequency loop only has to nullify the phase loop output to steer and confine the VCO [as \(F_c(s)\) has a pole at the origin] and hence \(\omega_c\). So \(I_f\) must be greater than the maximum average phase detector output

\[
I_f > \theta_{z\text{max}} K_{pd} I_p.
\]

Fast steering of the VCO at system startup, when \(C\) is discharged, is what is sacrificed by making \(I_f\) small. This fast steering at startup would not normally be a critical performance requirement. Providing

\[
\theta_{z\text{max}} K_{pd} < 1
\]

it is possible to choose \(I_f\) equal to \(I_p\). With \(I_f\) equal to \(I_p\), the frequency detector and phase detector outputs can be combined digitally (digital combiner Fig. 2) and only one charge pump is required.

### VI. Frequency Loop Filter

A possible system for implementing the disturbance reduction scheme outlined in the previous section, is to employ binary rate multipliers (BRM’s) [13] to produce the output pulses. Also, it is advantageous to include a pole \(\omega_p\) in the pulse spreading system, forming a low-pass filter. The digital low-pass filter limits the bandwidth of the frequency loop, helping to decouple it from the dynamics of the phase loop.

Operational digital techniques [13], can be used to provide an implementation of the pulse spreading system that also has the characteristics of a low-pass filter. The details of the development of a suitable binary Rate Multiplier based digital filter with one pole are given in the Appendix. The structure of the BRM-based digital filter is shown in Fig. 4.

### VII. Experimental Results for Sonet STS-3c Timing Recovery

The digital implementation of the SFPLL was used as the basis for a clock recovery system that meets SONET STS-3c specifications [6]. The SONET STS-3c clock recovery system was constructed using a field programmable gate array for the digital circuits. The VCO used was an integrated circuit multivibrator with a large gain \((K_0)\) of 106 MHz/V and a poorly specified free running frequency. A version has also been integrated in an application specific integrated circuit (ASIC). The digital integrated circuit developed included not only a clock recovery block based on the SFPLL described here, but also a range of other functions including SONET framing and asynchronous transfer mode (ATM) cell switching functions.
Experimental results on the performance of the clock recovery system are shown in Figs. 5 and 6. Fig. 5 shows that the SFPLL can be designed to limit the peaking in the transfer function to meet the standards requirement.

A version of the SFPLL which had the frequency loop bypassing $R$ and the output of the digital filter $[F_j(s)]$ feeding directly into the capacitor $C$ was built. This version requires two current pumps but the phase disturbance caused by pumping current through $R$ (17) is avoided. In Fig. 6 the reduction of frequency loop induced noise for the version which bypasses $R$ can be clearly seen.

VIII. CONCLUSIONS

The clock recovery system’s accurate output clock when no data input is present and accurate confinement are characteristics associated with expensive voltage controlled crystal-oscillator-based timing recovery systems. The SFPLL based clock recovery system provides voltage controlled crystal oscillator features at much lower cost. In addition it allows the phase loop bandwidth and range of frequencies to which the system will lock to be set freely. Voltage controlled crystal-oscillator-based timing recovery systems generally have very low bandwidth and a very limited range of frequencies to which they will lock. Additionally, different data rates can be accommodated with the same VCO by simply changing the reference frequency, or by adding an offset in the frequency loop.

A digital frequency loop delivers arbitrary precision in control of the SFPLL frequency, although it does introduce noise into the SFPLL output clock. Other SFPLL applications will typically have greater spectral purity requirements for the SFPLL output clock than timing recovery. Although, as can be seen from Fig. 6, the noise introduced by the digital frequency loop can be made small for a highly damped, narrow bandwidth loop.

For a class of SFPLL’s, the VCO phase noise can also be reduced [7]. In the implementation presented here this property was not invoked, as phase noise was not an issue for the particular application. For more demanding applications a large reduction in the phase noise of the SFPLL’s VCO can be achieved. However, a frequency detector more sophisticated than the rotational frequency detector is required.
APPENDIX

DEVELOPMENT OF A BRM BASED DIGITAL FILTER

In this appendix a BRM-based digital filter that has one pole is developed. BRM’s take an \( n \) bit binary number, \( B \) (between 0 and \( 2^n-1 \)), and produce an output pulse stream which has a ratio of ones to zeros given by

\[
\frac{B}{2^n} \tag{21}
\]

\( n \) is related to \( N_p \)

\[
N_p = 2^n. \tag{22}
\]

A single-pole system with input \( u(t) \) and output \( y(t) \) is described by the following differential equation:

\[
dy = \omega_p u(t) \, dt - \omega_p y(t) \, dt. \tag{23}
\]

A system of integrators and BRM’s that implements (23) is shown in Fig. 4. The BRM-based system runs off a clock of period \( N_p \frac{2\pi}{\omega_p} \). The integrator block accumulates the \( n \) bit value \( y(t) \), which is then fed into a BRM to produce the output pulse stream. The integrator block is implemented with an up–down pulse counter. The pulse stream from the frequency detector forms the input \( u(t) \, dt \). The fractional multiplier \( \omega_p' \) is assigned a value (24) so that the BRM based system has an identical time response as the system described in (23).

\[
\omega_p' = \omega_p N_p N_w \frac{2\pi}{\omega_0}. \tag{24}
\]

The output of the frequency detector is in pulse rate form and is fed directly into the system as \( u(t) \, dt \). Every increment in \( y(t) \) produces \( 1/\omega_p' \) pulses at the system output, before that increment in \( y(t) \) is nullified by a pulse at the negative input of the integrator block. To produce an increment in \( y(t) \) requires \( 1/\omega_p' \) pulses from the frequency detector. The pulse spreading scheme requires that \( N_p \) pulses be generated from every frequency detector pulse. \( N_p \) pulses from every frequency detector pulse.

Fig. 6. Spectrum of recovered timing (11 001 100 data pattern). (a) With resistor \( R \) in frequency loop. (b) Without resistor in frequency loop.
pulse can be achieved by either multiplying the input pulse rate by \( N_s \), or simply changing the fractional multiplier of BRM A \( \omega'_p \) to \( \omega'_p N_s \), i.e., do not divide by so much. The latter is the more preferable method, as no extra hardware is required. However, because the new fractional multiplier must be less than or equal to one, a new constraint is created

\[
\omega'_p N_s \leq 1, \quad (25)
\]

From (24) and (25) the following relating \( N_p \) to other system parameters is obtained

\[
N_p \leq \frac{\omega_0}{2\pi N_s N_{\alpha} \omega'_p}. \quad (26)
\]

If

\[
\omega'_p N_s = 1 \quad (27)
\]

then BRM A is eliminated and the frequency detector output is fed directly into the integrator. In general, as \( N_p \) has to be a power of two, \( \omega_p \) will have to be modified to satisfy (27)

\[
\omega_p = \frac{\omega_0}{2\pi N_s N_{\alpha} N_p}. \quad (28)
\]

REFERENCES


[11] Antonio Cantoni (M’74–SM’83–F’98) was born in Soliera, Italy, on 30 October, 1946. He received the B.E. (first class honors) and the M.Eng.Sc. degrees from the University of Western Australia in 1968 and 1972, respectively.

He was a Lecturer in computer science at the Australian National University, Canberra, in 1972. He joined the Department of Electrical and Electronic Engineering at the University of Newcastle, Shortland, NSW, Australia, in 1973, where he held the Chair of Computer Engineering until 1986. In 1987, he joined QPSX Communications Ltd, Perth, Western Australia, as Director of the Digital and Computer Systems Design Section for the development of the DQDB Metropolitan Area Network. From 1987 to 1990 he was also a Visiting Professor in the Department of Electrical and Electronic Engineering at the University of Western Australia. From 1992 to 1997 he was the Director of the Australian Telecommunications Research Institute and Professor of telecommunications at Curtin University of Technology, Perth, Western Australia. During this period he was also the Director of the Cooperative Research Center for Broadband Telecommunications and Networking.

He is currently Chief Technology Officer with Atmosphere Networks Inc., and Professor of telecommunications at the University of Western Australia. He is interested in adaptive signal processing, electronic system design, and networking and regularly acts as a Consultant to industry in these areas.

Dr. Cantoni is a Fellow of the Australian Academy of Technological Sciences and Engineering. He has been an Associate Editor of the IEEE TRANSACTIONS ON SIGNAL PROCESSING.