Design of a Unit Current Cell for a 12-bit 3.2GHz Current Steering Digital-to-Analog Converter

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Abstract

This thesis presents the design of a unit current cell for a 12-bit current steering Digital-to-Analog Converter (DAC) with 3.2GHz clock frequency. Some of the physical problems associated with the unit current cell design for a high speed current steering DAC are discussed in this thesis. The circuit is designed in Philips CMOS090, 90nm process, with a supply voltage of 1.2V. The design is based on a differential current steering topology. The differential output of the DAC is loaded with the two 25Ω resistor and a full-scale differential voltage of 0.5Vpp is generated.

The unit current cell is designed for a 5/7 thermometer/binary segmented DAC. The simulated DAC converts five most significant bits (MSBs) into the thermometer code, which controls the 31 unit current sources. The remaining 7 least significant bits (LSBs) control seven binary-scaled current sources. In this design a 5-bit (VHDL) binary/thermometer decoder is used.

Several current cell architectures are compared based on the physical problems associated with the current cell design. Cascoding is found to be the best option to overcome the error sources associated with the unit current cell design. However, the low supply voltage of 1.2V in CMOS090 limits the cascoding benefits. In this thesis, a new topology is presented to solve this low voltage headroom problem.
Introduction

The demand for high-speed Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) is increasing tremendously. DACs designed in CMOS technology are becoming more and more popular in high-speed communication, instrumentation and data acquisition system. During the past few years, the requirements of multiple carriers in CDMA, WCDMA and GSM systems mandated the use of a DAC, which provides the highest level of dynamic performance. In short the two performances like high conversion rate and high resolution are the key issues in the DACs design.

Current-steering DACs can be made with several different architectures. One of the freedoms is the segmentation, which is defined as a ratio between the thermometer code and the binary code part of the DAC. Another aspect of the architecture is a design of an individual current cell. In this thesis, the unit current cell design is implemented for a segmented architecture DAC. The design is simulated for the 5/7 thermometer/binary segmented current steering DAC. The goal is to explore a suitable current cell topology for a 12-bit DAC in CMOS090 90nm process in order to enhance the dynamic performance of the DAC. Designing of the unit current cell requires understanding of the error mechanisms, which influences the dynamic performance of the DAC. For the different current cell architectures the error sources have to be analyzed. The architecture choice for a unit current cell is made based on the analysis of the physical problems associated with the high-speed current steering DACs.

In chapter 1, the basic principles of digital-to-analog conversion are explained. Section 1.1 gives an overview of the most important performance definitions of the DACs. The different error sources associated with high-speed DACs are described in chapter 2. Main focus is on the physical problems associated with the unit current cell design. In chapter 3, the different current cell topologies are presented. Based on the error analyses, the different current cell architectures are compared. Chapter 4 presents a detailed design of the selected architecture. Finally, simulation results of the selected unit current cell design are explained in chapter 5 and conclusions are described in chapter 6.
1 Digital-to-Analog Conversion

Digital-to-analog conversion is an essential function in data processing systems. Digital-to-analog converters (DACs) generate an analog output (signal) that represents the digital input (signal). In this chapter different architectures of current steering digital-to-analog converters will be described and different kinds of properties of DACs will be discussed; e.g. INL and DNL error, Signal-to-Noise Ratio and Spurious Free Dynamic Range. These properties and architectures of a DAC determine its performance.

1.1 Performance definitions of Digital-to-Analog Converters

In high speed DACs, it is very important to characterize the performance in time domain but most of the characterization is done in the frequency domain. The characterizations can also be divided into static and dynamic properties. The static properties are given by settled values, and often too optimistic to determine the true performance of the DAC. The static performance is specified by the imperfections in four parameters: gain error, offset error, differential nonlinearity (DNL) and integral nonlinearity (INL). Output offset is defined as a constant dc offset in the transfer curve of analog output vs. digital input and therefore has no effect on frequency domain characterization. The gain defines the full-scale output of the DAC in relation to its reference circuit [1,2]. The DNL and INL static nonlinearities are explained in the next section. At higher frequencies the dynamic nonlinearities in the DACs overshadows the static nonlinearities (DNL and INL). The dynamic nonlinearities occur during the transition phase, they consist of glitches, time skew etc. [3]. In the following sections the most important properties of DACs will be discussed.

1.1.1 INL and DNL Error

![Figure 1.1 Non-ideal characteristic illustrating INL and DNL errors in a DAC](image-url)
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The INL expresses the deviation from the straight line as shown in figure 1.1. The ideal line is the ideal transfer function corrected for gain and offset errors. The DNL expresses how much the difference in output level between two adjacent codes deviates from the ideal LSB step $\Delta$. It is typically measured in least-significant bits (LSB). The INL is measured as maximum deviation from the best-fit line shown in figure 1.1. The DNL and the INL at step $k$ are defined by [4]

$$DNL_K = \frac{A_K - A_{K-1}}{a} \quad \text{and} \quad INL_K = \frac{A_K}{a\Delta}$$

Equation 1.1

where $a$ is the corrected input value for offset and gain error and $\Delta$ is the LSB step. Although the DNL and the INL are defined for all $k$, it is common to use the worst-case DNL and INL to express the quality of the converter. The worst-case DNL and the INL is given by,

$$DNL = \max_{k=0,\ldots,N} \{DNL_K\}$$

Equation 1.2

$$INL = \max_{k=0,\ldots,N} \{INL_K\}$$

Equation 1.3

From equation 1.1 the DNL and INL can be expressed as,

$$DNL_K = INL_K - INL_{K-1} \quad \text{and} \quad INL_K = INL_0 + \sum_{i=1}^{K} DNL_i$$

Equation 1.4

The INL and the DNL are good measures for identifying which bits that contain the largest error.

1.1.2 Harmonic distortion (HD$_k$)

The harmonic distortion with respect to the kth harmonic, HD$_k$, is the ratio of power between the kth harmonic and the fundamental, which is given by,

$$HD_k = 10 \cdot \log_{10} \frac{P_k}{P_1}$$

Equation 1.5

where $P_k$ is the power of the kth harmonic. $P_1$ is the power of the fundamental ($P_1 = P_s$ signal power). The total harmonic distortion (THD) is the ratio of the total harmonic distortion power and the power of the fundamental, i.e.
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\[ THD = 10 \cdot \log_{10} \frac{\sum_{k=2}^{\infty} P_k}{P_1} \] \hspace{1cm} \text{Equation 1.6}

Since, there is an infinite number of harmonics the THD is usually calculated using the first 10–20 harmonics or until the harmonics no longer can be distinguished from the noise floor [3].

1.1.3 Signal-to-Noise ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of the power of the fundamental and the total noise power within a certain frequency band, excluding the harmonic components, which is given by,

\[ SNR = 10 \log_{10} \frac{P_s}{P_n} \] \hspace{1cm} \text{Equation 1.7}

where \( P_s \) is the signal power and \( P_n \) is the noise power.

1.1.4 Signal-to-Noise and distortion ration (SNDR)

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the power of the fundamental and the total noise and distortion power within a certain frequency band, which is given by [5],

\[ SNDR = 10 \cdot \log_{10} \frac{P_s}{P_n + \sum_{k=2}^{\infty} P_k} \] \hspace{1cm} \text{Equation 1.8}

where \( P_s \) is the signal power and \( P_n \) is the noise power.

1.1.5 Spurious Free Dynamic Range (SFDR)

The spurious-free dynamic range (SFDR) is the ratio of the power of the fundamental component of the signal and the power of the largest spurious (unwanted) tone within a certain frequency band. SFDR is usually expressed in dB.

\[ SFDR = 10 \cdot \log_{10} \frac{P_s}{P_{\text{max}}} \] \hspace{1cm} \text{Equation 1.9}

where \( P_s \) is the signal power and \( P_{\text{max}} \) is power of the largest tone in the band of interest.
1.2 Architecture of Digital-to-Analog Converters (DACs)

There are different ways to convert a digital code into an analog output [1]. The architectures choice for DACs partly depends on the application. In all the different architectures, matched unit components such as resistors, capacitor or transistors are used to convert the digital input into the analog output. The design presented in this thesis uses a current steering architecture. Current steering DACs are much faster compared to the other architectures such as resistor ladder or capacitor architectures because it does not require an output buffer.

Current steering Digital-to-Analog Converters

The current steering architecture is suitable for high-speed and high-resolution applications, especially when special care is taken to improve the matching of the current sources. Conventional current-steering DACs are classified into two groups, a binary-weighted array and a unit current-cell matrix.

The basic principle of the current-steering DACs is to sum the currents from the current sources according to the digital input. The current steering DAC with a binary weighted architecture is shown in figure 1.2. The current sources are connected in parallel to each other. The current sources are connected to the output node via MOS switches, which are controlled by the input code. Therefore, the output current of the DAC is proportional to the input code.

![Binary weighted current-steering DAC](image)

Figure 1.2: Binary weighted current-steering DAC
1.2.1 Binary weighted DACs

In binary-weighted current-steering DACs the reference current $I_{ref}$, as shown in figure 1.2, is multiplied by powers of two, creating larger currents to represent the higher magnitude digital signal. Each switch switches a current to the output that is twice as big as the less significant bit. This means that the output current of the $k^{th}$ current source is equal to $2^{k-1} \cdot I_{ref}$, where $I_{ref} = I_{LSB}$ is the current of the least significant bit.

The advantage of this architecture is that it requires a relatively small area with a small number of transistors. This means that for a 12-bit converter there are only 12 current sources and an equal amount of switches. One more advantage of this architecture is its simplicity (no complex decoding logic). In the binary weighted architectures a special decoder is not required, because the binary input code can be directly applied to the switches. On the other hand, a large DNL error and an increased dynamic error are intrinsically linked with this architecture.

![Figure 1.3: (a) Glitch disadvantage for a binary-weighted DAC (b) Matching problems hurt the DNL performance](image)

In binary weighted DACs due to the large ratio between the LSB and the MSB, it is difficult to synchronize the switching. At mid-code transitions, $2^{N-1}$ unit current sources are switching on/off and $2^{N-1} - 1$ unit current sources are switching off/on (0111 $\leftrightarrow$ 1000). The output can change by substantially more than 1LSB, which gives rise to a glitch as shown in figure 1.3.a.
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Assuming a normal distribution for each current-source with the standard deviation of \( \sigma(I) \), then the mid scale step \( \sigma(\Delta I) \) is given by [6],

\[
\sigma(\Delta I) = \sqrt{2^{N-1} \sigma(I)} / I
\]

Equation 1.10

where \( I \) is the current switched by each current source and \( N \) is the number of bits. The sigma, \( \sigma(\Delta I) \), is a good approximation for the DNL error. The most significant bit (MSB) current source needs to be matched the sum of all the other current sources to within \( \frac{1}{2} \) LSB. Such matching can never be guaranteed because of the statistical spread. Therefore, this architecture is not guaranteed monotonic [6]. Matching is an issue for all bit transitions, but in the binary-weighted DAC the severity of the matching problem is determined by the weight of the bit, resulting in a typical differential nonlinearity (DNL) plot, as shown in figure 1.3.b. The matching of the MSB current source transistor must be extremely accurate because this limits the DNL performance of a binary-weighted DAC. Due to these mismatch and glitch problems, the full binary-weighted architecture does not exceed more than ten bits of resolution [1].

1.2.2 Thermometer DACs

Figure 1.4: Matching and glitch advantage of a thermometer-code DAC
In thermometer coded DACs, the digital input code is converted into a thermometer code, which controls the switches. As shown in figure 1.4.a, when the digital input increases by 1 LSB, one additional current source is turned on. Each current branch produces an equal amount of current, thus for N bit converter, \(2^N - 1\) current source and switches are required, which results in a larger area. Although unit-element arrays have the drawback of larger area than the binary weighted architectures, they also have the benefit of guaranteed monotonicity.

In addition, there are several other advantages for thermometer-coded DACs compared to binary weighted architecture DACs. The matching requirement in thermometer coded DACs is much relaxed: 50% matching of the unit current source is good enough for DNL < \(\frac{1}{2}\) LSB as shown in figure 1.4.b [2]. Thermometer coded DACs offer a lower glitch energy by minimizing the number of switched current cells at the mid-code transitions. The glitches hardly contribute to nonlinearity in thermometer coded DACs. This is because the magnitude of a glitch is proportional to the number of switches that are actually switching at a given sample time.

As shown in figure 1.4.c, when the step is small (i.e. one LSB changes), the glitch is extremely small, and when the step is larger (i.e. four LSBs change), the glitch is larger. However, as the number of switches that change is proportional to the size of the signal step, the magnitude of the glitch is directly proportional to the amplitude of the signal step. Thus the glitch does not cause any nonlinearity in the converter’s analog output signal.

The main disadvantages of the thermometer-coded approach are complex decoding logic, the large area requirement and high power consumption. For a 12-bit Digital-to-Analog converter the complete thermometer architecture is not suitable because as mentioned previously for N bit conversion, \(2^N - 1\) unit current sources are required. However, when the DACs specifications call for a high resolution as well as a good linearity and monotonicity, a combination of binary-weighted and unit-element arrays can be used to create a segmented digital-to-analog converter.

1.2.3 Segmentation

The combination of a thermometer coded and a binary weighted architecture is found in most of the DACs. This combination is called segmentation, where the DAC is divided into two sub DACs, one for the Most Significant Bits (MSBs) and the other for the Least Significant Bits (LSBs). The thermometer code is used for the MSBs and the binary weighted code is used for the LSBs. This is due to the thermometer-coded architecture giving good DNL and the binary-weighted DACs using less area.

The full binary weighted design means 0% segmentation and the full thermometer-code design means 100% segmentation. The obvious question that arises is how much to segment the converter (i.e. how many bits should be assigned for the thermometer part and how many for the binary-weighted part).
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Figure 1.5: a) Normalized required area versus percentage of segmentation b) THD versus percentage versus percentage of segmentation, (for 10-bit 500-Msample/s DAC in 0.35\mu m CMOS technology, [7])

The optimum segmentation point is determined as shown in figure 1.5(a). In [7], C. Hung Lin, et.al, has chosen the segmentation for a 10-bit converter. The DNL and MSB-LSB glitches versus required area and power determine the segmentation choice. As shown in figure 1.5.a, the area required for the 0\% segmentation is equal to $2^{10} \times A_{\text{Unit}}$, where $A_{\text{Unit}}$ is area of the unit current cell. This point is dominated by the size requirement to get a good DNL specification. As segmentation increases, the normalized area required decreases. However, at a normalized area of $2^6 \times A_{\text{Unit}}$ the INL requirement becomes the limiting specification, for both the binary and the thermometer code architectures. The INL requirement is independent for a certain degree of segmentation, which is indicated by the horizontal line in figure 1.5.a.

In the thermometer-coded approach extra decoding logic is needed for each current source, hence the decoding logic demanded by the thermometer-coded section begins to dominate, with an area equal to $2^M \times A_{\text{decode}}$, where $A_{\text{decode}}$ is the area of the digital decoding logic in each current source cell and $M$ is the number of bits in the MSB section. The digital logic area becomes more dominant in the size of the converter because the numbers of current sources increase exponentially with a higher percentage of segmentation. It is clear from the above plot (Figure 1.5.a), that any point on the horizontal line would be an optimum level of the segmentation. However, the glitch performance of the thermometer code architecture is better than of the binary weighted. The glitch problems with binary weighted coding give rise to the total harmonic distortion (THD).

As explained in section 1.2.1, the binary weighted architecture DACs give the glitches at the mid-code transition and the total harmonic distortion is proportional to the nonlinear glitch energy. Thus, the more bits that are contained in the LSB section, the higher the glitch energy, as shown in figure 1.5.b.
Therefore, according to the theory in [7], the optimal degree of segmentation occurs at the rightmost part of the horizontal line in the plot, which is still a minimum area and meets the DNL specification, and has the smallest THD. The MSB-LSB glitches are important to determine the optimal segmentation level, but there are other sources of errors, which also determine the optimal segmentation. The maximized segmentation can cause problems such as complex logic and large number of switching elements. The thermometer coding does not improve the skew between the switches; this means that a higher degree of segmentation can result in worse time skew [8].
2 Error Analysis of Current Steering DACs

In this chapter, a number of dynamic issues will be discussed. The performance of the DAC is limited due to various causes. Some of the main errors, which are limiting the performance, are listed below [3].

- **Matching error**: The variation in the process forces the oxide thickness threshold voltage, transistor widths, etc., to vary over the chip area. Due to the mismatch error, the identically designed transistors become unmatched, which affects the linearity of DAC.
- **Finite output impedance**: The finite output impedance of the unit current source strongly affects the linearity of the converter. This is mainly caused by the non-ideal current source having a finite output impedance, which is signal dependent.
- **Settling time error**: A limited settling time will cause the settling error, which can be signal dependent and hence introduce distortion. The settling errors occur due to the parasitic capacitances within the current sources.
- **Charge feedthrough**: Due to the capacitive coupling between gate and drain of the current switch, charge or current will be induced in the output terminal of the DAC.
- **Glitches**: due to the nonideal switches, different capacitive loads on different bits and matching errors, there will be a time skew between the bits. This will introduce the current or voltage spikes at the output, which are called glitches.

2.1 Matching Error

Mismatch is the process that causes time-independent random variation in the physical quantities of identically designed devices (current sources) [9]. The physical quantities such as the oxide thickness, threshold voltage, transistor width etc. varies over the chip area during the creation process. Due to the matching error, identical designed transistors become unmatched.

The matching determines the accuracy of the current source. The influence of the matching errors makes the sizes of the transistors to differ from their designed values, therefore the output current will not be correct. A current source with a mismatch error can be modeled as an additional current source in parallel with the nominal current source [4].
Chapter 2. Analysis of Current Steering DACs

Figure 2.1 A model of the current source with error current source, $\Delta I_u$

It is assumed that the $2^N-1$ unit current sources are used to define the current source shown in figure 2.1. Also, in this case, the ideal output current is given by $\tilde{I}_u = I_u$. Each unit current source has an absolute matching error equal to $\delta I_u$. Hence, the actual output current will be

$$I_u = \tilde{I}_u + \delta I_u$$  \hspace{1cm} \text{Equation 2.1}

The relative matching error is given by

$$\varepsilon_u = \frac{\delta I_u}{I_u}$$  \hspace{1cm} \text{Equation 2.2}

The matching errors are assumed to be statistically independent and Gaussian distributed with zero mean and variance, equal to $\sigma_u^2$. Hence, the SNDR can be found by taking the ratio between the signal power and the matching plus noise error power. The SNDR and SFDR for an N-bit converter are given by [5].

$$\text{SNDR} \approx 6.02 \cdot N + 1.76 - 10 \cdot \log_{10}(1 + 3 \cdot \sigma_u^2 \cdot 2^{N+1}) \text{dB}$$  \hspace{1cm} \text{Equation 2.3}

$$\text{SFDR} \approx 3 \cdot (N + 3) - 10 \cdot \log_{10} \sigma_u^2 \text{ dB}$$  \hspace{1cm} \text{Equation 2.4}
In equation 2.4 the 3rd harmonic distortion is considered. From equation (2.3) it is clear that for low mismatch values the SNDR reaches its ideal value, which is determined by $SNDR = 6.02 \cdot N + 1.76 dB$ [1].

2.2 Finite output impedance

A finite output impedance of the current source strongly affects the linearity of the converter. If the output (current summing) node of the current-steering array, as shown in figure 2.2, experiences a large voltage excursion then the nonlinearity arises due to the finite output impedance of the current sources [1].

![Generalized model of a differential mode binary-weighted DAC.](image)

Figure 2.2 Generalized model of a differential mode binary-weighted DAC.

The output resistance of the DAC is a function of the number of switched on current cells, thus depends on the input signal. In addition to that, the DAC output has a capacitive nature due to the current source switches and interconnections. The output capacitance of the current source is also signal dependent. Therefore the time constant of the output signal is modulated by the input code. The effects of the output conductance and capacitance variation are described in the next sections.
Output conductance variation

If a current source is made with transistors then the output conductance of the current source is not zero. Transistors are dependent on the applied voltage across them i.e. the voltage across the drain and source, and hence, they will have a finite output impedance.

![Diagram of a current source with non-zero output conductance](image)

Figure 2.3 (a) gives a generalized model of the current source and its non-zero output conductance. The output conductance associated with the unit current source is assumed to be $G_{\text{unit}} = \frac{1}{R_{\text{unit}}}$ and the total output conductance of the DAC is given by,

$$G_{\text{out}} = G_{\text{unit}} \cdot \text{code}$$  \hspace{1cm} \text{Equation 2.5}

Equation 2.5 shows that the output conductance $G_{\text{out}}$ is input code dependent; it will give rise to a signal dependent gain, i.e. distortion. Hence, the performance of the DAC depends on the conductance ratio, $\rho$ [5].

$$\rho = \frac{G_{\text{unit}}}{G_{\text{Load}}} = G_{\text{unit}} \cdot R_{\text{Load}}$$  \hspace{1cm} \text{ Equation 2.6}

where $G_{\text{Load}} = \frac{1}{R_{\text{Load}}}$ is the load conductance.
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The SFDR of the DAC for a full-scale signal is equal to [4],

\[
SFDR = \left[1 + \frac{1}{\rho \cdot 2^{N-1}} \cdot \sqrt{1 + 2^N \cdot \rho}\right]^2
\]

Equation 2.7

where \(N\) represents the number of bits. The SFDR is strongly dependent on the conductance ratio. If \(\rho\) is very small then the SFDR can be approximated by,

\[
SFDR \approx -20 \log_{10} \rho - 6(N - 2)
\]

Equation 2.8

From equations 2.6 and 2.8, it seems that by doubling the load resistance, the SFDR is decreased by 6dB. Equation 2.8 shows that the linearity is also distorted with an increased nominal number of bits. The SNDR for a full-scale sinusoid input can be also expressed as a function of the conductance ratio by [4].

\[
SNDR = \frac{1}{6\rho \left(2^{N-1} \cdot \left(1 + \frac{1}{8}\right)\right)}
\]

Equation 2.9

in dB this is equal to,

\[
SNDR = -6(N - 0.4) - 20 \log_{10} \rho \ dB.
\]

Equation 2.10

The error caused by the non-ideal output conductance can be compensated by using a transimpedance amplifier (output buffer) as shown in figure 2.4, which provides the DAC with a virtual ground and hence a low impedance load.

![Diagram](image)

Figure 2.4 Conversion of output current of an array to voltage using (a) resistor and (b) transimpedance amplifier
As shown in figure 2.4.a, the single resistor $R_L$ converts the output current to a voltage. In this case, node $X$ experiences the entire output voltage swing and this topology suffers from the limited output impedance error. This problem can be avoided, as shown in figure 2.4.b, by placing the resistor $R_L$ in the feedback loop around the op-amp $A_I$, which provides a virtual ground at node $X$. As a result, the voltage variation at node $X$ is quite small and modulation of output impedance is small. The settling time of the DAC is determined by the op amp's speed. However, the buffer itself may limit the performance of the DAC. There are various trade-offs among speed, linearity, output voltage swing and driving capability of the op-amps that often restrict the dynamic range and settling speed of the DAC [10]. In this design, simple output cascode switch is used.

Output capacitance variation

The output capacitance of the DAC is a function of the input code just like the output resistance. In this section, the output capacitance variation problem is viewed as a time domain error. The time domain errors are dominating at higher frequencies [11]. The signal dependent output capacitance and the resistance modulate the settling time of the DAC.

![Figure 2.5 The modulation of output capacitance by input code.](image)

The variation in the output capacitance can be modeled as shown in figure 2.5, where $C_u$ is the output capacitance of the unit current cell and $w$ represents the input code. Hence, the output capacitance of the DAC, $C_{out}$, linearly depends on the input signal.

$$C_{out}(w) = w \cdot C_u + C_L \quad \text{Equation 2.11}$$

The output capacitance of the unit current source, $C_u$, changes when the switch is turned on or off. The output capacitance as a function of state of the switch is shown in figure 2.6.
Figure 2.6 Output capacitance depends on the switch state.

When the switch is off, the output capacitance of the current cell is equal to $C_{\text{off}}$. If the switch is turned on the capacitance will be $C_{\text{on}}$. The unit capacitances $C_u = C_{\text{on}} - C_{\text{off}}$ is the difference between the on and off state capacitance. Thus the total output capacitance, $C_{\text{out}}$, for a thermometer coded DAC is given by [11].

\begin{equation}
C_{\text{out}} = C_L + C_u \cdot w + (2^{N-1}) C_{\text{off}}
\end{equation}

where $N$ is the number of thermometer bits. The load capacitance $C_L$ and the fixed capacitance $(2^{N-1}) C_{\text{off}}$ are independent of the input signal. As a result, the difference in on and off state capacitance, $C_u$ is very important because it gives rise to the signal dependent errors.

There are several problems caused by the fact that the output capacitance is a function of the input code. The first problem is the signal dependent rise/fall time and the second problem is the charge feedthrough.

2.2.1 Modulation of rise and fall time

The signal dependent settling time is caused by the variation in the output capacitance and resistance of the DAC, which will result in a data dependent rise/fall time. When a current source is off, it has an infinite resistance and a capacitance, which depends on the size of the current switch. But when the switch turns on, the capacitance is slightly changed by adding a capacitance, $C_u$. As explained in the previous section, the total output capacitance of the DAC is equal to $C_{\text{out}} = C_L + C_u \cdot w + (2^{N-1}) C_{\text{off}}$; where $C_u \cdot w$ is code dependent. The output resistance of the DAC is a function of the input signal, which is given by $R_o \equiv R_u / w$; where, $w$ represents the input code. Hence, the settling time of the DAC can be approximately given by [12],

\begin{equation}
\text{Equation 2.12}
\end{equation}
\[ \tau(w) = R_L \cdot C_L + R_L C_u \cdot w = \tau_0 + \tau_u \cdot w \quad \text{Equation 2.13} \]

where \( \tau_u \cdot w \) more important, because every extra current cell that is switched on, increases the time constant by \( \tau_u \), whereas \( \tau_0 \) is constant.

One solution to this modulation of the output capacitance and resistance is the use of buffer at the output node, which buffers the current at this output node (virtual ground), as shown in figure 2.4. In this case, the modulation of the output impedance of the DAC is significantly reduced. The main drawback of this approach when the aim is to use the DAC for a high speed and a high accuracy application is that the buffer should be more linear than the overall DAC. This buffer limits the speed and dynamic range of the DAC at higher frequencies.

### 2.2.2 Charge feedthrough

Charge feedthrough is another physical problem, which affects the performance of the DAC. The amount of charge injected into the output node depends on the number of switched on current sources. The charge-feedthrough is related to the parasitic coupling between the gate and the drain of the MOS switches.

![Figure 2.7 Charge feedthrough in a current steering DAC](image)

The charge feedthrough phenomenon is explained in figure 2.7. The current from the unit current source is switched between the two output branches through the MOS switches. The switching is controlled by the applied switching signal. The charge appears at the output node through the capacitive coupling between the gate and drain of the switches.
During switching, the charge passes from the switch control node to the output node of the DAC through the gate-drain overlap capacitance, \( C_{gd} = W_s C_{ov} \), where \( C_{ov} \) is the overlap capacitance per unit width, \( W_s \) is the width of the switch transistor.

The charge is a function of the size of the switch devices (size relates to capacitance), the control signal swing and the slope of the driving signal [13]. The charge injected in the output node is given by,

\[
Q = V_{in} W_s C_{ov} \tag{2.14}
\]

where \( V_{in} \) is the swing of the switch-driving signal. This charge injection results in a voltage error at the output node, which is approximately equal to [11],

\[
\Delta V \approx V_{in} \frac{\Delta N \cdot C_{gd}}{C_L + C_{gd} + C_{out}} \tag{2.15}
\]

where \( \Delta N \) is the number of switched on current sources and \( C_{out} \) is the output capacitance of the DAC, which changes by the applied input code.

As described in section 2.1, the output capacitance of the DAC is given as \( C_{out} = C_u \cdot w + (2^{N - 1}) C_{off} \), where, the difference in on-off state capacitance \( C_u \) is more important. When \( C_u \) is assumed to be zero then the output capacitance of the unit current cell would not depend on the input code word applied to the DAC. The signal applied to the current source switches is differential in nature. The charge injected in one output node is opposite to the charge injected in the other.

When the capacitance \( C_u \) is assumed to be nonzero, as is the case in this design, then the \( C_u \) depends on the input code and the charge is not perfectly compensated. Therefore, there exist two different error mechanisms due to the charge feedthrough. In the first, the error contribution is due to the fact that each switched on current source introduces some amount of charge in the output terminal of the DAC. This error results in nonlinearity in the DAC, because the number of the switched on current sources depends on the input signal. The second error mechanism appears via the charge to voltage translation at the output node of the DAC. This voltage variation modulates the output impedance, which affects the performance of the DAC.

There are various methods presented in literature for reducing the effect of charge feedthrough. In this design cascoded switches are used, which will be described in chapter 4.
2.3 Timing error

The size of the switches (size is related to the capacitance) and slope of the driver signal determine the timing accuracy of the DAC. For calculating the timing accuracy of the DAC, the current source cell and driver circuit is considered.

![Figure 2.8 Timing error with unit current cell and driver](image)

As shown in figure 2.8, the unit current source switches are driven by the driver circuit, which has a current equal to $I_d$. The capacitance of the current source switch is given by

$$C_s = W_s L_s \cdot C_{ox}$$  \hspace{1cm} \text{Equation 2.16}

where $W_s$ is the width of the switch and $L_s$ is the length. $C_{ox}$ is the gate-oxide capacitance of the switch. The capacitance at the output of driver is determined by the contributions of the self-load capacitance of the driver $C_d$ and the gate capacitance, which is expressed as,

$$C_{total} = C_s + C_d$$  \hspace{1cm} \text{Equation 2.17}
For this calculation the driver is assumed ideal, such that there is no timing spread caused by the driver capacitance, $C_d$. As the switches are driven by the constant switching signal, the capacitance at the output of the driver is charged and discharged with the constant current, $I_d$. Hence, the slope of the driving signal is given by [14]

\[
S = \frac{I_d}{C_{\text{total}}}
\]

Equation 2.18

where $S$ is the slope of the switching signal for single ended signal and for differential case the slope is two times larger. The offset voltage of the MOS differential pair can be written as,

\[
\sigma_{\text{offset}} = \frac{A_{V\text{TH}}}{\sqrt{W_s L_s}}
\]

Equation 2.19

where $A_{V\text{TH}}$ is a process parameter in $\text{mV} \cdot \mu \text{m}$, which characterizes the threshold voltage properties of the used CMOS process, and $W_s, L_s$ are the dimensions of the switches. If we assume that the gate capacitance $C_s$ domines, then the spread of the timing error is equal to,

\[
\sigma(\Delta t_s) = \frac{\sigma_{\text{offset}}}{S} = \frac{A_{V\text{TH}}(W_s \cdot L_s \cdot C_s + C_d)}{I_d \sqrt{W_s L_s}}
\]

Equation 2.20

The timing error spread is inversely proportional to the driver current and linearly proportional to the area of the switch. This means that when the device size is increased, the timing error increases due to the extra capacitance. For a small timing spread, $\sigma(\Delta t_s)$, the slope of the switching signal needs to be steep. The large slope requires a large driver current, $I_d$ and a small capacitance, i.e. small switches. But the smaller switch means a larger offset voltage, therefore a larger timing spread.

Hence, to minimize the effect of the timing spread error the slope of the driver signal has to be very steep that means a large $I_d$. The large current needs a large size transistor, hence more area. In addition to that, for smaller offset voltage a large switch transistor is required, which results in more charge feedthrough. The large output capacitance also modulates the settling time of the DAC.
Summary

The error analysis associated with the current steering DACs is presented. Mainly the errors associated with the unit current cell were taken into account. The performance of the DAC is affected by the finite output impedance. The code dependent output resistance and capacitance modulates the settling time of the DAC. The code dependent output capacitance also contributes to the charge feedthrough error, which will affect the performance of the DAC. The charge injected in the output node is translated into a voltage step, which will modulate the output impedance of the DAC.

The variation in the output conductance can be compensated with the help of a transimpedance amplifier (output buffer). However, this buffer would introduce other problems, which would limit the performance of the DAC.
3 Architecture Choice for a Unit Current Cell

In this chapter the different unit current cell architectures are described and compared. The focus is to explore a suitable unit current cell topology for the 12-bit DAC in Philips CMOS090, 90nm process.

The main part of current steering DACs is a unit current source. The unit current source has a large influence on the performance of current steering DACs. In current steering DACs the integral nonlinearity (INL) is mainly affected by the matching behaviour of the current sources. The matching of the current sources is one of the main issues in high-speed, high-resolution DACs design. The performance of the DACs is mainly limited by three factors: 1) voltage fluctuation of the output node of the current source due to improper timing of switching off and on of the switch transistor; 2) charge feedthrough into the output terminal; 3) imperfect synchronization of the control signal of the current switching transistors [15]. The unit current source needs to be designed with care to avoid the problems listed above. In this chapter, the first two error sources are taken into account and the charge feedthrough phenomenon was described in chapter 2.

3.1 Basic unit current cell

The basic unit current cell, as shown in figure 3.1, consists of a single MOS transistor as a current source and two switching transistors. The switching transistors are directly exposed to the output terminal of the DAC i.e. the global output node, where such a 2^n-1 current cells are connected. Hence, this circuit topology is mainly subjected to all three errors listed above.

![Figure 3.1 Basic unit current Cell (no cascode)](image)
Voltage fluctuation:

Ideally, the voltage at the output node of the current source should be constant. In reality, the switching causes a significant voltage variation at node $A$, in figure 3.1. The voltage variation at the drain of the current source transistor makes the current source transistor to drop out of saturation. A large current source transistor is used for matching purposes, which results in a large parasitic capacitance. This current source parasitic capacitance is one of the main sources of errors. While switching, the current source transistor drops out of saturation, the parasitic capacitor of the current source discharges and it takes time to charge again. This charging/discharging will increase the settling time of the DAC. Therefore, it affects the dynamic performance of the DAC.

![Voltage Fluctuation Diagram](image)

**Figure 3.2** A voltage fluctuation at common node

Figure 3.2 shows the simplest differential control signals applied to the switches of the current source in figure 3.1, which varies between 0V and $V_{DD}$. The crossing point of the two control voltages is $V_c = V_{DD}/2$. Therefore the voltage variation at the common node, $A$ is given by [15],

$$
\Delta V = -\frac{V_{DD}}{2} + \left( \sqrt{\frac{2I}{\beta}} - \sqrt{\frac{I}{\beta}} \right) \approx 0.5V
$$

Equation 3.1

where, $I$ is the current of the unit current source and $\beta = (W_s/L_s)KP$ and $KP$ is the gain of the transistor.

Thus, there is a significant voltage variation at the drain of the current source. The capacitance at the common node discharges due to this voltage variation. Therefore, two scenarios can occur. In the first scenario, the capacitance $C_s$ discharges rapidly and the voltage at the common node follows the voltage change at the switching transistor. Therefore, the voltage at the drain of the current source transistor drops and the unit current source enters the linear region. In the second scenario, the capacitance
Chapter 3. Architecture Choice for a Unit Current Cell

$C_S$ discharges slowly and the unit current source remains in saturation but the settling-time of the DAC increases.

There are several methods proposed in literature to avoid the errors due to the voltage fluctuation at the common node. One of the common circuits is a current source with a cascode configuration [16].

3.2 The cascode configuration current cell

A cascode configuration is used to isolate the current source transistor from the voltage fluctuation at the common node. As shown in figure 3.3, a small sized cascode transistor is used to shield the large current source transistor.

![Figure 3.3 The cascode configuration current cell](image)

The current cell with cascode configuration topology isolates the current source from the voltage variation at the common node. The small size cascode transistor implies small parasitic capacitance. Due to this small parasitic capacitance the problems caused by the voltage fluctuation are reduced and the settling time of the DAC is improved.

The cascode configuration current cell results in a high output impedance, which positively affects the linearity of the DAC. This is, because the maximum relative non-linearity (INL) of a DAC is approximately given by $N R_L / 4 r_o$ [1], where $R_L$ is the load resistance of the DAC and $r_o$ is the output impedance of the unit current cell. However, these benefits of cascoding are only possible if the cascode configuration transistor remains in saturation.

The low voltage headroom i.e. lower supply voltage of the CMOS090 process limits the use of a cascode configuration. On top of that this topology also suffers from the charge feedthrough problem. The charge feedthrough at the output is correlated with the input signal. The amount of charge injected in the output terminal depends on the number of switching current cells. As described in chapter 2, the charge feedthrough
is code dependent. Each turned on current cell induces a certain amount of charge in the output terminal. The charge induced through the gate–drain capacitive coupling between the control signal node and the output of the DAC is translated in a voltage step at the output, which affects the dynamic performance of the DAC.

There are various methods presented in the literatures to reduce this charge feedthrough effect. One possible way to reduce the charge feedthrough is to isolate the switching transistor from the output terminal of the DAC [16].

3.3 The cascode configuration current cell with cascoded switches

As shown in figure 3.4, two cascode transistors, M3 and M4 are used to isolate the switching transistors from the output node of the DAC. The cascoded switch transistors are stacked on top of the switching transistors.

![Figure 3.4 The cascode configuration current cell with cascoded switches](image)

This topology reduces the charge feedthrough significantly by isolating the current switches from the output node of the DAC. The cascode current source transistor isolates the current source transistor from the voltage fluctuation at node $A$ and also improves the output impedance of the unit current cell. All the benefits of cascoding are possible provided that the current source transistor remains in saturation. However, with the low voltage headroom in the CMOS090 process, it is difficult to achieve benefits of cascoding. The voltage headroom is not sufficient to keep the current source in saturation.

One solution to achieve all the benefits of the cascoding even with the lower supply voltage is by replacing the cascode transistors by thick oxide layer transistors, which can operate with higher voltages up to 3.3V.
3.4 The cascode current cell with thick oxide layer cascoded switch

The low voltage headroom problem in CMOS090 can be solved using a thick oxide layer transistor for the output cascode switch cascode, as shown in figure 3.5.

![Figure 3.5 The current cell with thick oxide layer cascoded switch transistor](image)

This thick oxide layer transistor increases the voltage headroom significantly because it can operate with higher supply voltages. However, care should be taken to prevent the voltage at the drain of the switching transistors from increasing beyond the maximum supply voltage of CMOS090 technology, i.e. 1.2V. As shown in figure 3.5, the output voltage 1.8V, hence to keep the voltage at node 1 below 1.2V an auxiliary current source is used. The output cascoded switch can shield the switch transistor from the output node of the DAC, only if it remains in saturation. Hence, the auxiliary current sources are used to keep the output cascode transistors in saturation. Moreover, these extra biasing current sources result in a complex circuitry and increased power.

The current cell with the thick oxide layer cascoded switches improves the voltage headroom significantly, hence the benefits of cascoding, such as reduced charge feedthrough and shielding of the current source transistor from voltage fluctuation at the common source node is possible. However, the auxiliary currents are required to bias the thick oxide transistors.
3.5 Comparison of different current cell architectures

All the described current cell architectures have positive and negative effects on the DAC performance. Therefore, a fair comparison between all these architectures is made based on some simulation results in order to select a suitable architecture. In this section, the different current cell approaches are taken into account and a suitable topology for CMOS090 is explored. All these topologies are compared mainly based on the physical problems associated with the current steering DACs such as the signal dependent output capacitance, the settling time error and charge feed through in the output terminal of the DAC.

A. Code dependent output capacitance

The output capacitance depends on the input code, just like the output resistance. The capacitance of the unit current cell changes when the switch is turned on and off. This change in the capacitance is modeled as shown in figure 2.6 in chapter 2.

When a switch is off, the off state capacitance is equal to \( C_{\text{off}} = C_{gd} + C_{db}(v) \), where \( C_{gd} \) is the gate drain overlap capacitance of the switch and \( C_{db}(v) \) is its drain-bulk junction parasitic, which is voltage dependent. When the switch is turned on, the output capacitance is equal to \( C_{\text{on}} = C_{gd} + C_{db}(v) + C_{\text{channel}} \), where \( C_{\text{channel}} \) is the channel capacitance of the switch transistor. Hence, the total output capacitance for the thermometer DAC is given by [11],

\[
C_{\text{out}} = (2^N - 1)\left(C_{gd} + C_{db}(v)\right) + w \cdot C_u
\]

Equation 3.2 shows two signal dependent errors, one is due to the voltage dependent drain-bulk junction capacitance, \( C_{db}(v) \) and the other is due to the difference in the on/off state capacitance (\( \Delta C \)). The voltage dependent drain-bulk capacitance depends on the dimensions of the switch transistor. Therefore, use of a small sized switch transistor easily reduces the associated errors.

The output capacitance of the current cell depends on the output voltage of the DAC, i.e. the number of turned on current cells. The difference in the on/off state capacitance (\( \Delta C \)) is more important than the absolute value of the output capacitance. Hence, in figure 3.6 the difference in on/off state capacitance is plotted as a function of output voltage for the different current cell topologies.
The smaller the difference between the off and on state capacitance, the smaller the error of the capacitance modulation by the input code, this was described in more detail in chapter 2. It is visible from figure 3.6, that the current cell with the thick oxide layer cascoded switches topology has a smaller capacitive difference at the lower output voltages compared to the other three topologies. Hence, with the other three current cell architectures the full-scale output current of 20mA is not possible. On the other hand, the current cell with the thick oxide cascoded switches improves the voltage headroom sufficiently such that the benefits of cascoding are achievable.

The settling time of the DAC is also modulated due to the signal dependent output capacitance of the unit current cell. The modulation of settling time will be described in the next section.

B. Settling time error

In figure 3.7, the difference in the settling time of the unit current cell with an accuracy of 12-bit is plotted for the current cell with and without thick oxide cascoded switches. The settling time is the time required for the DAC to reach the final value within the accuracy of the DAC. The difference in the settling time is also a function of the output voltage. The output resistance of the DAC is code dependent as well as the output capacitance of the DAC is a function of output code; therefore the settling time of the DAC is also modulated by the input code.
Chapter 3. Architecture Choice for a Unit Current Cell

Figure 3.7 The settling time difference plotted as a function of the output voltage

It is visible from figure 3.7, that the settling time difference is large at full-scale output current of 20mA (i.e. 0.7V) for the current cell architectures without thick oxide layer cascoded switches. If the difference in the on/off states capacitance is large, then the settling time of the DAC also increased due to the large capacitance. Therefore, at low output voltages, the dynamic performance of the DAC is affected due to the modulation of the settling time. On the other hand, the current cell with the thick oxide layer transistor shows smaller on/off state capacitive difference compared to the other current cell architectures, which results in smaller settling time error.

C. Charge feedthrough

As explained in chapter 2, another effect of the signal dependent output capacitance is charge feedthrough, which affects the performance of the DAC. The charge injected into the output node depends on the number of switched on current cell. The charge feedthrough is related to the parasitic coupling between the gate and the drain of the current switches. The charge induced in the output terminal without thick oxide cascode switch is approximately equal to 1fC and with thick oxide cascode switches the charge feedthrough is reduced to 0.65fC.

Hence, the current cell with thick oxide cascoded switch architecture reduces the charge feedthrough significantly and gives small on/off state capacitive difference, which results in smaller settling time. Table 3.1 gives detail comparison of the different unit current cell architectures.
Chapter 3. Architecture Choice for a Unit Current Cell

Table 3-1 Comparison of different unit current cell architectures

<table>
<thead>
<tr>
<th>Current Cell Architecture</th>
<th>Charge feed through</th>
<th>Output Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DC (R_o)</td>
</tr>
<tr>
<td>Basic CC (figure 3.1)</td>
<td>1.2fC</td>
<td>77 MΩ</td>
</tr>
<tr>
<td>Cascode configuration CC (figure 3.3)</td>
<td>1 fC</td>
<td>81 MΩ</td>
</tr>
<tr>
<td>Cascode CC with cascoded switch (figure 3.4)</td>
<td>0.87fC</td>
<td>130 MΩ</td>
</tr>
<tr>
<td>Cascode CC with thick oxide cascoded switch (figure 3.5)</td>
<td>0.65fC</td>
<td>163 MΩ</td>
</tr>
</tbody>
</table>

Table 3-1 Comparison of different unit current cell architectures

Summary

The different unit current cell architectures were observed in order to explore a suitable unit current cell topology for the CMOS090 process. To compare the different architectures a number of analysis were performed. The focus was mainly on the error sources related to the unit current cell, such as the charge feedthrough, the output capacitance variation and the settling time error. The comparison of architectures shows that the basic current cell topology suffers from all three errors mentioned above. The cascode configuration current cell with cascoded switch reduces the charge feedthrough and isolates the current source transistor from the voltage variation at the common node. However, the low supply voltage in CMOS090 limits the benefits of cascoding. Moreover, this low voltage headroom problem was solved using thick oxide cascoded switches but it requires extra biasing.
4 Design of a Unit Current Cell

In this chapter, a unit current cell design is presented for a 12-bit digital-to-analog converter. The design is based on the architecture choice described in the previous chapter. The unit current source is designed in a CMOS090 process with a supply voltage of 1.2V.

4.1 Design goals and design specifications

The goals of the design are to analyze the effects of the error sources described in chapter 2 and to see the effects of different current cell topologies on the performance of the DAC. The design is based on the architecture choice made in chapter 3, i.e. the current cell with the thick oxide layer cascoded switches.

This unit current cell is designed for the 5/7 thermometer/binary segmented current steering architecture, which consists of input buffers, a 5-bit binary-to-thermometer decoder, master-slave latches, delay equalizers, current switch drivers and current cell. All these sub-circuits are shown in figure 4.1. However, the focus is on the current cell design. The unit current cell consists of the current source, current source switches and output cascode switches. A short description of the design specification is given in table 4.1.
### Table 4-1 Design specification

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>3.2GHz</td>
</tr>
<tr>
<td>Signal frequency</td>
<td>600MHz</td>
</tr>
<tr>
<td>Full scale current</td>
<td>20mA</td>
</tr>
<tr>
<td>LSB current</td>
<td>≈ 5μA</td>
</tr>
<tr>
<td>Unit current</td>
<td>625μA</td>
</tr>
<tr>
<td>Driver current</td>
<td>200μA</td>
</tr>
<tr>
<td>Load</td>
<td>25Ω</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS090</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2V</td>
</tr>
<tr>
<td>SFDR</td>
<td>60-65dB (frequency - 600MHz)</td>
</tr>
</tbody>
</table>

#### 4.2 Design considerations

In this section, some practical design considerations concerning the choice of the circuit elements in a unit current cell design are explored. The different building blocks of the current steering DAC are given in figure 4.1. Most essential are the current source and the current switches. In the following sections, the unit current source and the current switch are described in detail.

#### 4.2.1 Unit current cell

The schematic of the unit current cell used in this design is shown in figure 4.2. It consists of a cascoded current source and a thick oxide layer cascoded switch pair. A short list of the parameters of the unit current cell design is given in table 4.2.

![Figure 4.2 Schematic of realized current cell](image)
Chapter 4. Design of a Unit Current Cell

### Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>( W/L )</th>
<th>( I_{\text{unit}} )</th>
<th>( W_s/L_s )</th>
<th>( \Delta V_{\text{swing}} )</th>
<th>( W_{TS}/L_{TS} )</th>
<th>( I_{\text{auxi}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current source</td>
<td>48.32(\mu m)/16(\mu m)</td>
<td>625(\mu A)</td>
<td>10.5(\mu m)/0.1(\mu m)</td>
<td>0.4(V)</td>
<td>8.5(\mu m)/0.4(\mu m)</td>
<td>6(\mu A)</td>
</tr>
<tr>
<td>Cascode current source</td>
<td>28.32(\mu m)/0.28(\mu m)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unit current</td>
<td>( I_{\text{unit}} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current switch</td>
<td>( \Delta V_{\text{swing}} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control signal swing</td>
<td>( W_s/L_s )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cascode switch</td>
<td>( W_{TS}/L_{TS} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Auxiliary current</td>
<td>( I_{\text{auxi}} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4-2 Design parameters

The focus is on the error sources associated with the unit current cell and their effects on the dynamic performance of the DAC. The unit current source must be designed with care, because the dynamic performance of the DAC is mainly affected by the matching of the unit current source. For a 12-bit resolution DAC, the unit current source needs to be accurate and fast enough to achieve the desired specifications.

The issues considered during the design of the current source are the matching of the current source transistors, the current source transistor isolation and the signal dependent output impedance and nonlinear settling. These issues are described in detailed in this section.

**Matching of the current source**

To achieve 12-bit accuracy in the converter, the currents of the individual thermometer current sources should be very well matched and the binary one should be scaled according the thermometer current source. Matching is one of the key issues in the design of high-speed resolution DACs. Based on the size versus matching relation [9] for MOS transistors an expression for a unit current source area is given by [15],

\[
(WL) = \frac{1}{2} \left[ A_p^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)} \right] \left( \frac{\sigma(I)}{I} \right)^2
\]

where \( A_{VT}^2 \) and \( A_p^2 \) are mismatch process parameters and \( (V_{GS} - V_T) \) is the gate overdrive voltage. Equation 4.3 shows that for a given area of the unit current source, i.e. \( W = 48.32\mu m \) and \( L = 16\mu m \) the calculated standard deviation of a unit current source, \( \frac{\sigma(I)}{I} \) is equal to 138\(nA\).
For the current steering DACs, the INL is mainly determined by the matching behavior of the current sources. Due to this mismatch, the INL specification of the different DACs made in the technology varies randomly. A parameter, which is introduced for expressing this technology versus DAC-specification, is the INL yield. This INL yield is defined as a ratio of the number of D/A converter with an INL smaller than $1/2$ LSB to the total number of tested D/A converters. Assuming a normal distribution of the unit current sources, the required accuracy on the current source is given by [4]

\[
\text{INL} \approx \sqrt{2^N \left( \frac{\sigma(I)}{I} \right)^2} \text{ LSB}
\]  
Equation 4.2

\[
\frac{\sigma(I)}{I} \leq \frac{1}{2C\sqrt{2^N}}, \text{ where, } C = \text{norm}^{-1}\left(0.5 + \frac{\text{yield}}{2}\right),
\]  
Equation 4.3

\(\text{\sigma(I)/I}\) \hspace{1cm} \text{standard deviation of a unit current source,}
\(N\) \hspace{1cm} \text{number of bit of DAC,}
\(\text{norm}^{-1}\) \hspace{1cm} \text{inverse cumulative normal distribution,}
\(\text{yield}\) \hspace{1cm} \text{relative number of DACs with INL < 1/2 LSB.}
Current source transistor isolation

One of the problems associated with the unit current cell is the large parasitic capacitance at the drain of the current source transistor. The solution for this problem is presented in figure 4.3.b and figure 4.3.a shows the current cell without cascode.

![Figure 4.3 a) no cascode b) single cascode](image)

As mentioned in section 3.1, the current cell without cascoding suffers from all three physical problems. This is mainly due to the fact that the current source has a large parasitic capacitance at node $A$. The capacitance at node $A$ is determined by the capacitance of the switches and the capacitance of transistor $M_1$. The current source transistor, $M_1$ is large due to the matching requirements, which results in a large parasitic capacitance. While switching, this parasitic capacitance discharges, as a result $M_1$ drops out of saturation and the capacitance needs to charge again. If this happens it takes a long time to re-enter in saturation. This charging and discharging of the parasitic capacitance increases the settling time of the DAC.

In this design, the cascode transistor, $M_2$ is used to isolate the large parasitic capacitance of the current source transistor, $M_1$. A small size cascode transistor, shields the large current source transistor from the voltage fluctuations at the common node. The small transistor means a small parasitic and small settling time. This cascode transistor also increases the output resistance of the DAC.
Signal dependent output impedance and Non-linear settling

The next problem associated with the unit current source is the output impedance modulation based errors such as a signal dependent settling time and frequency dependency of the current cell output impedance. These errors are caused by the capacitance present at the inner nodes of the current cell. Some circuit details of these problems with the current cell shown in figure 4.4.a.

As described, in section 3.5, when a switch is turned off, (for example $M_{S1}$ is on and $M_{S2}$ is off) the capacitance seen at the output of $M_{S2}$ is equal to $C_{off} = C_{gd} + C_{db}(V)$ and at the output of the $M_{S1}$ is equal to $C_{on} = C_{gd} + C_{db}(V) + C_{u}$, where $C_{gd}$ is the gate-drain overlap capacitance and $C_{db}(V)$ is the voltage dependent drain bulk capacitance. This capacitive difference in on/off state of the switches is code dependent, which also modulates the settling time of the DAC. This on/off state capacitive difference modulation is compensated with the simple cascoding switches, as shown in figure 4.4(b). With the cascode transistor the change in the impedance is reduced. Hence, the settling time of the DAC is more constant.
4.2.2 Current switches

The switches steer the current from the current source in the differential output branches. The critical design parameters for the switch are its width and length dimensions and the shape of the driving signal, including slope and voltage swing. The switch needs to be sized carefully because it addresses the charge feedthrough phenomena and the signal dependent modulation of the switch common source node.

As described in section 2.2, the charge feedthrough phenomena are in the first order proportional to the channel and gate drain overlap capacitance of the switch and to the swing of the switch control signal. The capacitance and the control signal swing determine the amount of charge injected into the output terminal of the DAC and the slope of the driver signals determines how fast the charge is deposited. However, a small swing of the switch control signal, a small switch size and a small slope can reduce the charge feedthrough.

Charge compensation

The second solution to the charge feedthrough problem is to compensate it. The charge can be compensated with the use of dummy switch transistors [17], which are driven by a complimentary driving signal. These dummy switch transistors of half width (W/2) dimension are switching in parallel with the switching transistors. As shown in figure 4.5, the dummy transistor gate is connected to the complimentary control signal; therefore, the net charge injected is reduced.

![Figure 4.5 Charge compensation by using dummy switches](image)

However, this solution has drawbacks: the charge compensation only works for a symmetrical control signal and the control signal is deliberately made asymmetrical. The switching speed will be affected because the dummy transistor loads the driver circuit. Another method of compensating the charge feedthrough is the use of transmission gates [14]. This transmission gates consist of a pMOS connected in
parallel with a nMOS transistor. The charge feedthrough will cancel out since the pMOS transistor absorbs the charge that the nMOS transistor induces into the output terminal. The influence on the conductance is low for the pMOS transistor, with the same dimensions as the nMOS transistor. Therefore, the speed is lower. Moreover, the pMOS switch increases the parasitic capacitance, giving relatively low frequency pole at the output node. This reduces the dynamic performance of the DAC. Hence, in this design the dummy transistors are not used.

*Cascode switches*

One of the solutions for reducing the charge feedthrough is to decouple the switch output node from the DAC output node. This can be achieved with a global (buffer or trans impedance amplifier, figure 2.4) or a local buffer. The use of single (global) buffer in the DAC output has several drawbacks [10]. Hence, it is not used in this design. The local buffering offers advantages, because each current cell is buffered locally, and there is no need for a high linearity global buffer to handle large current at the high frequencies. This can be realized with the nMOS cascode transistors, as shown in figure 4.6.

This cascode switches isolate the switches from the output node of the DAC. For a Low to High transition of the control signal, the voltage variation at the output is, $\Delta V_{out} = 0V$, because the related cascode transistor is cut off and the path between the output node and drain of the switching transistor is open. On the other hand, for a High to Low transition, the related cascode transistor is in saturation, and the voltage fluctuation at the source of the cascode transistor is small because it is a low impedance node. Hence, the voltage fluctuation at the source node of the cascode transistor is given by [18]
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\[ \Delta V_D = \frac{1}{g_{m_{cas}}} C_{gd(sw)} \frac{\Delta V_{in}}{t_f} \]  

Equation 4.4

where \( C_{gd} \) is the gate-drain capacitance of the switching transistor and \( t_f \) is fall time of the control signal. With this methodology the charge feedthrough is not completely compensated but it is reduced. The \( g_{m_{cas}} \) of the cascode transistors determines the amount of charge to be absorbed, i.e. it depends on the size of the cascode switches. Apart from the charge reduction, it reduces the change in the impedance seen from the switches. As mentioned in chapter 2, the output impedance is code dependent. The cascode transistor gives nearly constant impedance; therefore the signal modulated settling time error is also small.

In this design, the thick oxide layer transistor is used as a cascode transistor. This thick oxide transistor can operate with higher voltages up to 3.3V. While designing the thick oxide cascode transistor, care should be taken that its source voltage should not increase beyond the maximum supply voltage of the CMOS090 process. Hence, the thick oxide transistor needs to be biased well. For limiting the source voltage below 1.2V an auxiliary current source is used.

Spikes at common switch node

Ideally, the voltage at the drain of the current source transistor should be constant. But, in reality the switching causes voltage fluctuation. As shown in figure 4.7.a, this switching signal is generated a simple driver circuit. The main reason for the voltage fluctuation at the common node is the level of the crossing point of the differential driver signal. With the simplest switch control signal varying between Vdd and 0V, the voltage fluctuation at the common node is approximately 0.5V; see section 3.1. Due to this voltage variation, the current source parasitic capacitance discharges and needs to charge gain. This will influence the setting time of the DAC.

There are three methods to raise the crossing point of the control signal, which are shown in figure 4.7:

1. The first method is to delay the driver signal, as shown in figure 4.7.b.
2. The second method is to delay the rising or the falling of the control signals, as shown in figure 4.7.c.
3. In the third method, figure 4.7.d, the crossing point is raised with reducing the voltage swing of the control signal. The output voltage of the driver is changed in such a way that the lower output voltage is higher than zero.
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The first two methods are not used because in the first method, the delaying of the control signal limits the use of a high clock frequency and the method of different rise or fall time reduces the speed [14]. In this design the third method is used, where the voltage swing is reduced with the help of increasing the $V_{off}$ voltage. If the lower output voltage is increased, the switching point of control signal is also increased. This method has advantage of the low swing. The reduced swing results in a reduced charge feedthrough. However, the slope of the control signal is reduced at the crossing point, which negatively affects the timing spread. In this design a 400mV voltage swing is selected.

Summary

The unit current cell design was presented in this chapter. In this design a combination of the cascode current source and the thick oxide layer cascode switches are used. Due to the cascode current source the output impedance of the current cell increases. Moreover, the switches are not directly coupled to the large parasitic capacitance of the current source transistor. Hence, the settling time decreases. The thick oxide layer output cascode switches solve the voltage headroom problem of the CMOS090 process and shield the current switches from the output node of the DAC. The output node voltage and the impedance change according to the input code. With the output
cascode switches the current switches are isolated from these changes. The settling time of the switches is less dependent on the input code. Therefore, the dynamic performance of the DAC increases.
5 Results

In chapter 4, the circuit implementation of the current cell was presented. This current cell design was simulated and the results are described in this chapter. The design is made in CMOS090, a 90nm process, with a supply voltage of 1.2V. Aim of the design is to see the effect of unit current cell architecture on the performance of the DAC. The simulated DAC has a resolution of 12-bit. The unit current cell design can operate at a clock frequency of 3.2GHz and a simulated input frequency of 600MHz.

In the following sections, a comparison between the selected current cell architecture and the other current cell architectures is presented. Also the error analyses of the selected architecture (the cascoded current source with thick oxide cascoded switch) are presented. The effect of the selected circuit parameters on the dynamic performance (SFDR) of the DAC is described.

5.1 Signal dependent output capacitance

![Figure 5.1 The capacitance as a function of the output voltage on the output node of the unit current cell with the thick oxide output cascode.](image)

The output capacitance of the unit current cell is a function of the output voltage. In figure 5.1, the output capacitance is plotted versus the output voltage for the cascode current cell with thick oxide cascoded switches. The output capacitance depends on the state of the current switch. The above plot shows that when switch is off, the output capacitance of the unit current cell is equal to 9fF (when output voltage = 1.8V). On the other hand, the on state output capacitance is equal to 19fF for the full-scale.
output current of 20mA, i.e. 1.3V. The difference in the on/off state output capacitance is more important than the absolute value of this capacitance.

The unit current cell with thick oxide cascode transistors has a smaller capacitive difference at the full-scale output current (20mA i.e. 1.3V) compared to the other current cell topologies. The comparison was given in section 3.5. In following graph, the output capacitive difference is plotted for the current cell (cascoded current source) with and without thick oxide output cascode.

![Graph showing output capacitive difference for current cell with and without thick oxide output cascode.](image)

Figure 5.2 $\Delta C$ plotted for a current cell (CC) with thick oxide layer output cascode and for a CC without output cascode.

As shown in figure 5.2, the current cell without output cascode shows a smaller difference between on/off state output capacitance, $\Delta C$ at lower output voltages. Hence, this current cell topology can be used only when the output voltage swing is smaller or equal to 0.3V. However, for this current cell $\Delta C$ is equal to 50fF at the specified full-scale output current of 20mA (i.e. output voltage swing of 0.5V). Hence, with this topology the full-scale output current of 20mA is not possible.

On the other hand, the thick oxide cascoded switches current cell shows a smaller difference in the on/off state output capacitance, i.e. 10fF at the full-scale output current of 20mA. Therefore, due to this smaller $\Delta C$ the error caused by the signal dependent output capacitance is also small.
5.2 Charge feedthrough reduction with thick oxide output cascode switches

In figure 5.3, the output currents of the current cell with and without thick oxide cascode switches are plotted. The effect of the output cascode is visible in the above plot. Due to the output cascode the charge injection is significantly reduced. The charge induced in the output terminal without cascode switch is equal to $1\mu C$ and with cascode switches the charge feedthrough is reduced down to $0.65\mu C$. The amount of charge compensated depends on the size of the output cascode transistors. The effect of the output cascode transistor will be explained in section 5.4.2.
5.3 Voltage fluctuation the output of current source

As shown in figure 5.4.a, the voltage fluctuation at the drain of the current source transistor without the cascode current source is equal to 80mV. On the other hand, figure 5.4.b shows the voltage variation is reduced to 10mV with the help of cascode current source transistor. Hence, with the help of the cascode transistor the current source transistor is shield from the voltage fluctuations at the common source node of the switches. The settling time of the DAC is also improved due to the small size cascode current source transistor.
5.4 Error source analysis

In the following plot, the performance (SFDR) of the DAC is plotted versus the input frequency. As shown in figure 5.5, at the lower input frequencies a SFDR up to 80dB is achievable. On the other hand, at higher frequencies i.e. especially the interested band of frequencies (600MHz-1GHz) the SFDR is limited between 66 to 60dB.

![Figure 5.5 SFDR versus input frequency](image)

Several tests are performed to analyze the error sources, which are limiting the performance of the DAC at higher signal frequencies. As shown in figure 5.6, extra capacitances are added to investigate the dominating error source in the unit current cell.
The effects of extra capacitance at the gate-drain of the current switches \((C_{gd})\), at the common source node of the switches \((C_{cs})\) and at the output of the current switches \((C_{out})\) are plotted in figure 5.7.a. In figure 5.7.b, the integer multiples of the initial (schematic level parasitic capacitance) values of the capacitance \(C_{gd} (2\text{fF})\), \(C_{out} (19\text{fF})\) and \(C_{cs} (18\text{fF})\) are plotted versus the performance. In these simulations, an ideal driver is used to switch the current switches. The driver current, \(I_{driver} = 200\mu\text{A}\) is used and the voltage swing of the control signal is 0.4V.
Figure 5.7 a) Effect of extra \( C_{gd} \), \( C_{cs} \) and \( C_{out} \) on the DAC performance b) Effect of integer multiple value of the \( C_{gd} \), \( C_{cs} \) and \( C_{out} \) on the performance of the DAC\(^1\)

\(^1\) Note: Initial (schematic-level parasitic) value of the \( C_{gd} = 2 \)\(^{fF} \) for the switch size of \( W_s/L_s = 10.5/0.15 \) \( \mu m \), the on state capacitance of the unit current cell, \( C_{out} = 19\)\(^{fF} \) and \( C_{cs} = 18\)\(^{fF} \) for the cascode current source transistor size equal to \( W/L = 28/0.28\) \( \mu m \).
Figure 5.7.a. and figure 5.7.b. show that the effect of the gate-drain overlap capacitance, $C_{gd}$, dominates. The schematic-level parasitic capacitance value of $C_{gd\,(ov)}$ is 2fF, for a switch size equal to $W_s/L_s = 10.5\mu m/0.15\mu m$. It is clear from figure 5.7.a that the performance curve starts rolling off at $C_{gd\,(ov)} = 2fF$. The performance (SFDR) is affected due to the large gate-drain overlap capacitance.

5.4.1 Effects of the small $C_{gd}$ and driver current on the performance

The small switch size and the small voltage swing of the switch control signal favour the charge reduction. In this design, the control signal voltage swing was selected as 0.4V and the switch size is $W_s/L_s = 10.5\mu m/0.15\mu m$ ($C_{gd\,(ov)} = 2fF$). One of the possible solutions to reduce the charge feedthrough is to use a small size switch transistor, i.e. small gate-drain overlap capacitance, $C_{gd\,(ov)}$. To check the effect of a smaller gate-drain overlap capacitance (smaller than 2fF) of the switching transistor, a simulation test was performed with negative values of $C_{gd}$ (2fF + additional negative value). The simulation result is presented in figure 5.8.

![Figure 5.8 Effects of small $C_{gd}$ and boosted driver circuits.](image)

As shown in figure 5.8 (curve 1), the DAC performance can be improved up to 70dB, if the gate-drain overlap capacitance of the switch is smaller than 2fF. A large size current switch means a large gate-drain overlap capacitance and that results in increased charge injection in the output terminal of the DAC. Hence, the dynamic performance of the DAC is mainly affected by the charge feedthrough error.
Curve 2, in figure 5.8 shows the effect of the driver current on the performance of the DAC. The driver current is increased from 200μA to 400μA. As shown in figure 5.7, the performance is improved by increasing the driver current, because a large driver current results in a large slope and hence, small timing spread. However, with the increased driver current the performance of the DAC also starts degrading for $C_{gd}$ equal to 2fF.

5.4.2 Effect of output cascode on the performance of the DAC

In this design, the output cascode transistors are used to isolate the drains of the switching transistors from the voltage fluctuation at the global output node of the DAC. The output cascode transistor source is a low impedance point. Hence, the voltage variation at the inner node of the current source is very small. In this section, a test is proposed to analyze the effect of the output cascode transistor on the performance of the DAC. The test results are not fully investigated at this moment. The test schematic is shown in figure 5.9, where the output cascode is buffered from the drain of the current switch transistor and applying a fixed voltage to the drain of the switches.

![Test schematic for output cascode](image.png)

Figure 5.9 Test schematic for output cascode
As shown in figure 5.9, the drain voltage of the switch transistor is fixed at 0.72V i.e. the drain voltage of the turned on switch transistor and the same current is copied into the corresponding output cascode transistor by a current controlled current source. This test shows that for the fixed voltage (0.72V) at the drain of the switch transistor the performance was improved to 72dB. The performance versus the drain voltage of switching transistor is plotted in figure 5.10.

![Figure 5.10 SFDR versus drain voltage of switch transistor](image)

As shown in figure 5.10, if the voltage at the drain of the switch transistor is increased towards 1.2V i.e. off voltage of the switch, then the performance is degraded. The causes of this performance degradation are not this moment clear. However, this simulation shows that a small voltage variation at the drain of the switch transistor results in better performance. This indicates that the output cascode needs to be design in such a way that the inner node of the unit current cell will experience smaller voltage variations.
6 Conclusions

The problems associated with the current cell design in CMOS090 process were taken into account and the different current cell architectures were analyzed. The different current cell topologies were compared based on the physical problems associated with high-speed DACs. The analyses were performed mainly for the output resistance and capacitance modulation of the unit current cell, charge feedthrough and modulation of the settling time. The comparison based on these analyses showed that each current cell architecture has advantages and disadvantages.

The basic current cell architecture (figure 3.1) suffers from all three errors such as charge feedthrough, voltage fluctuations at the common source node and the signal dependent output impedance modulation. This is, because the current source switches are exposed to the dynamic output node of the DAC. In the cascode configuration current cell (figure 3.3), the current source transistor is shielded from the voltage variation at the common source node of the switches. The cascode current source transistor also improves the settling time of the DAC. However, this current cell architecture suffers from the charge feedthrough error. The cascode current source with the cascoded switches architecture (figure 3.4) is one of the possible solutions for reducing the charge feedthrough. However, the benefits of the cascoding are limited due to the low voltage headroom in CMOS090. Hence, a new current cell topology was explored to resolve this low voltage headroom problem associated with the CMOS090 process. In this new approach thick oxide layer transistors were used as output cascode. These thick oxide output cascode transistors improved the voltage headroom and showed better performance at a full-scale output current of 20mA.

A circuit application of the selected unit current cell architecture (figure 3.5) has been presented. The circuit is based on a 12-bit DAC with 5/7, thermometer/binary-segmented architecture. In this DAC, the cascoded current source with the thick oxide cascoded switch was used. The thick oxide output cascode transistors solve the limited voltage headroom problem in CMOS090. The thick oxide transistors can operate up to 3.3V but care should be taken that the voltage headroom at the drain of the switching transistors is limited below 1.2V. In this design, an auxiliary current of 6μA was used to limit the voltage. Hence, the new current cell topology increased the voltage headroom significantly, but it requires an additional biasing current.

The unit current cell with thick oxide cascoded switches can operate with a 3.2GHz clock frequency. At 3.2GHz clock frequency and a signal frequency of 600MHz the SFDR is equal to 66dB and at low signal frequencies the SFDR is equal to 80dB.

Numbers of analyses were performed to investigate the error source, which is limiting the performance at high signal frequencies. The output impedance of the DAC is code dependent and at the higher frequencies the modulation of the output capacitance is more dominating than the output resistance. From the analyses results, it can be concluded that the charge feedthrough mainly affects the dynamic performance of the
DAC. The charge feedthrough depends on the size of the switches and the voltage of the node where the charge is injected.
7 Recommendations

In order to have benefits of cascoding, the voltage headroom should be sufficient to keep current source transistor in saturation. The use of the current cell architecture with cascoded current source and cascoded switches (figur3.4) is limited in CMOS090 process due to the low voltage headroom. One of the possible ways to improve the headroom is, to reduce the output load resistance of the DAC. However, by changing the load resistance the signal power is changed. The DAC output is connected through a 1:1 transformer to a 50Ω load (0.5V voltage swing). Hence, with a proper choice of transformer ratio and reduced output load resistance of the unit current cell the voltage headroom can be increased without changing the output signal power.

The effect of charge feedthrough, on the performance of the DAC is required to be investigated in detail. During the layout of the design, special attention should be paid to the gate-drain overlap capacitance of the current switches.

During the design of the output cascoded switches the care should be taken in sizing the output cascode transistors and setting the proper value of the auxiliary current, within an optimum trade-off.

The effect of the cascoded switches on the performance of the DAC should be investigated further.
8 Appendix

In this chapter, the circuit implementations are presented.

8.1 Circuit Implementation of the DAC

Figure 8.1 Implementation of the DAC
8.2 Circuit implementation of the master latch and buffer

![Figure 8.2 Implementation of the master latch and buffer](image)

8.3 Circuit implementation of the slave latch

![Figure 8.3 Implementation of slave latch](image)
8.4 Circuit implementation of the current cell and the driver

Figure 8.4 Implementation of the unit current cell and driver
References


