Simulating Turing Machines on Maurer Machines

J.A. Bergstra$^{1,2}$ and C.A. Middelburg$^3$

$^1$ Programming Research Group, University of Amsterdam,
P.O. Box 41882, 1009 DB Amsterdam, the Netherlands
janb@science.uva.nl

$^2$ Department of Philosophy, Utrecht University,
P.O. Box 80126, 3508 TC Utrecht, the Netherlands
janb@phil.uu.nl

$^3$ Computing Science Department, Eindhoven University of Technology,
P.O. Box 513, 5600 MB Eindhoven, the Netherlands
keesm@win.tue.nl

Abstract. Maurer machines are much closer to real computers than
Turing machines. Computer instructions play a prominent part in Mau-
er machines. It illustrates that the instruction implicitly
executed by a Turing machine on a test or write step must be capable of
reading or overwriting the contents of any cell from the infinite number
of cells on the tape of the Turing machine. Real computers do not have
such instructions. We show two ways to get rid of this kind of infinity.

Keywords: Turing machines, Maurer machines, thread algebra, stored
threads, strategic interleaving, thread forking, fair interleaving strategies.


1 Introduction

In [12], Maurer proposes a model for computers that is quite different from the
well-known models such as register machines, multistack machines and Turing
machines (see e.g. [9]). The strength of Maurer’s model is that it is close to real
computers. Computer instructions play a prominent part in his model.

In [4], we developed a theory which covers basic issues concerning stored
threads and their execution. In that paper, we showed among other things that
a single thread can control the execution on a Maurer machine of any finite-
state thread stored in the memory of the Maurer machine, provided the basic
actions of the stored thread correspond to instructions of the Maurer machine.

To describe threads, we used an extension of BTA (Basic Thread Algebra),
introduced in [2] under the name BPPA (Basic Polarized Process Algebra). BTA
is a form of process algebra which is tailored to the description of the behaviour
of deterministic sequential programs under execution. The extension concerns an
operator for interleaving of threads and, for each Maurer machine, an operator
for applying a thread to the Maurer machine from a state of the Maurer machine. Applying a thread to a Maurer machine amounts to a sequence of state changes according to the instructions that the Maurer machine associates with the basic actions performed by the thread.

In this paper, we show a straightforward way to simulate Turing machines on a Maurer machine. It illustrates that the instruction implicitly executed by a Turing machine on a test or write step must be capable of reading or overwriting the contents of any cell from the infinite number of cells on the tape of the Turing machine – the cell of which the contents is actually read or overwritten depends on the head position. In Maurer’s terminology, a test instruction has an infinite input region and a write instruction has an infinite output region. Real computers do not have such instructions. We show also that the instructions concerned can be replaced by instructions with a finite input region and a finite output region if we abandon the restriction to machines with a finite-state control.

In the straightforward way to simulate Turing machines on a Maurer machine, a thread applied to the Maurer machine corresponds to the finite-state control of the Turing machine in question. This thread is definable by a finite recursive specification. However, the adaptation of this way to simulate Turing machines to the use of instructions with a finite input region and a finite output region usually leads to a thread that is only definable by an infinite recursive specification. Thus, in the simulation of Turing machines just as well, one kind of infinity has been replaced by another kind. We show a way to get around the latter kind of infinity in the case of convergent computations. The basic ideas are: (a) the thread corresponding to the finite-state control of the Turing machine in question is stored and then executed under control of a thread that makes the head position part of the instructions and (b) the controlling thread grows, by means of thread forking, whenever a head position occurs for the first time. For this, the operator for interleaving of threads from [4] is adapted to thread forking. This operator is based on the simplest deterministic interleaving strategy, namely cyclic interleaving. In [3], other plausible interleaving strategies are treated. We discuss why the last-mentioned way to simulate Turing machines on a Maurer machine works for other fair interleaving strategies as well.

The structure of this paper is as follows. First of all, we review Maurer’s model for computers (Section 2) and Basic Thread Algebra (Section 3). Following this, we extend BTA with an operator to deal with interleaving of threads (Section 4) and, for each Maurer machine, an operator which allows for threads to transform states of the associated Maurer machine by means of its instructions (Section 5). After that, we set out a way to store a finite-state thread in the memory of a Maurer machine for execution on the Maurer machine (Section 6). Next, we review Turing machines (Section 7) and show a simple way to simulate Turing machines on Maurer machines (Section 8). Then, we show two ways to simulate Turing machines on Maurer machines by means of instructions with a finite input region and a finite output region only (Sections 9 and 10). After that, we discuss why the latter way, which uses cyclic interleaving, works for any fair interleaving strategy (Section 11). Finally, we make some concluding remarks (Section 12).
2 Maurer Computers

In this section, we shortly review Maurer computers, i.e. computers as defined by Maurer in [12].

A Maurer computer $C$ consists of the following components:

- a set $M$;
- a set $B$ with $\text{card}(B) \geq 2$;
- a set $S$ of functions $S : M \to B$;
- a set $I$ of functions $I : S \to S$;

and satisfies the following conditions:

- if $S_1, S_2 \in S$, $M' \subseteq M$ and $S_3 : M \to B$ is such that $S_3(x) = S_1(x)$ if $x \in M'$ and $S_3(x) = S_2(x)$ if $x \notin M'$, then $S_3 \in S$;
- if $S_1, S_2 \in S$, then the set $\{x \in M \mid S_1(x) \neq S_2(x)\}$ is finite.

$M$ is called the memory, $B$ is called the base set, the members of $S$ are called the states, and the members of $I$ are called the instructions. It is obvious that the first condition is satisfied if $C$ is complete, i.e. if $S$ is the set of all functions $S : M \to B$, and that the second condition is satisfied if $C$ is finite, i.e. if $M$ and $B$ are finite sets.

Let $(M, B, S, I)$ be a Maurer computer, and let $I : S \to S$. Then the input region of $I$, written $IR(I)$, and the output region of $I$, written $OR(I)$, are the subsets of $M$ defined as follows:

$IR(I) = \{x \in M \mid \exists S_1, S_2 \in S, y \in OR(I) \bullet \forall z \in M \setminus \{x\} \bullet S_1(z) = S_2(z) \land I(S_1)(y) \neq I(S_2)(y)\},$

$OR(I) = \{x \in M \mid \exists S \in S \bullet S(x) \neq I(S)(x)\}.$

$OR(I)$ is the set of all memory elements that are possibly affected by $I$; and $IR(I)$ is the set of all memory elements that possibly affect elements of $OR(I)$ under $I$.

Let $(M, B, S, I)$ be a Maurer computer, let $I \in I$, let $M' \subseteq OR(I)$, and let $M'' \subseteq IR(I)$. Then the region affecting $M'$ under $I$, written $RA(M', I)$, and the region affected by $M''$ under $I$, written $AR(M'', I)$, are the subsets of $M$ defined as follows:

$RA(M', I) = \{x \in IR(I) \mid AR(\{x\}, I) \cap M' \neq \emptyset\},$

$AR(M'', I) = \{x \in OR(I) \mid \exists S_1, S_2 \in S \bullet \forall z \in IR(I) \setminus M'' \bullet S_1(z) = S_2(z) \land I(S_1)(x) \neq I(S_2)(x)\}.$

$AR(M'', I)$ is the set of all elements of $OR(I)$ that are possibly affected by the elements of $M''$ under $I$; and $RA(M', I)$ is the set of all elements of $IR(I)$ that possibly affect elements of $M'$ under $I$.

In [12], Maurer gives many results about the relation between the input region and output region of instructions, the composition of instructions, the decomposition of instructions and the existence of instructions. In [4], we summarize the main results.
3 Basic Thread Algebra

In this section, we review BTA (Basic Thread Algebra), a form of process algebra which is tailored to the description of the behaviour of deterministic sequential programs under execution. The behaviours concerned are called threads.

In BTA, it is assumed that there is a fixed but arbitrary set of basic actions $A$ with $\tau \not\in A$. We write $A_{\tau}$ for $A \cup \{\tau\}$. BTA has the following constants and operators:

- the deadlock constant $D$;
- the termination constant $S$;
- for each $a \in A_{\tau}$, a binary postconditional composition operator $\bowtie_a \bowtie$.

We use infix notation for postconditional composition. We introduce action prefixing as an abbreviation: $a \circ p$, where $p$ is a term of BTA, abbreviates $p \bowtie_a \bowtie p$.

The intuition is that each basic action performed by a thread is taken as a command to be processed by the execution environment of the thread. The processing of a command may involve a change of state of the execution environment. At completion of the processing of the command, the execution environment produces a reply value. This reply is either $T$ or $F$ and is returned to the thread concerned. Let $p$ and $q$ be closed terms of BTA. Then $p \bowtie_a \bowtie q$ will proceed as $p$ if the processing of $a$ leads to the reply $T$ (called a positive reply), and it will proceed as $q$ if the processing of $a$ leads to the reply $F$ (called a negative reply). The action $\tau$ plays a special role. Its execution will never change any state and always produces a positive reply.

BTA has only one axiom. This axiom is given in Table 1. Using the abbreviation introduced above, axiom T1 can be written as follows: $x \bowtie_\tau \bowtie y = x \bowtie_\tau \bowtie x$.

<table>
<thead>
<tr>
<th>Table 1. Axiom of BTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$x \bowtie_\tau \bowtie y = x \bowtie_\tau \bowtie x$</td>
</tr>
</tbody>
</table>

A recursive specification over BTA is a set of equations $E = \{X = t_X \mid X \in V\}$, where $V$ is a set of variables and each $t_X$ is a term of BTA that only contains variables from $V$. We write $V(E)$ for the set of all variables that occur on the left-hand side of an equation in $E$. Let $t$ be a term of BTA containing a variable $X$. Then an occurrence of $X$ in $t$ is guarded if $t$ has a subterm of the form $t' \bowtie_a \bowtie t''$ containing this occurrence of $X$. A recursive specification $E$ is guarded if all occurrences of variables in the right-hand sides of its equations are guarded or it can be rewritten to such a recursive specification using the equations of $E$. We are only interested in models of BTA in which guarded recursive specifications have unique solutions, such as the projective limit model of BTA presented in [1, 2]. A thread that is the solution of a finite guarded recursive specification over BTA is called a finite-state thread.

We extend BTA with guarded recursion by adding constants for solutions of guarded recursive specifications and axioms concerning these additional constants. For each guarded recursive specification $E$ and each $X \in V(E)$, we add
Table 2. Axioms for guarded recursion

\[
\langle X | E \rangle = \langle t_X | E \rangle \quad \text{if} \ X = t_X \in E \quad \text{RDP}
\]

\[
E \Rightarrow X = \langle X | E \rangle \quad \text{if} \ X \in V(E) \quad \text{RSP}
\]

Table 3. Approximation induction principle

\[
\begin{align*}
\pi_0(x) &= D & \text{P0} \\
\pi_{n+1}(S) &= S & \text{P1} \\
\pi_{n+1}(D) &= D & \text{P2} \\
\pi_{n+1}(x \sqsubseteq a \sqsupseteq y) &= \pi_n(x) \sqsubseteq a \sqsupseteq \pi_n(y) & \text{P3} \\
(\bigwedge_{n \geq 0} \pi_n(x) = \pi_n(y)) & \Rightarrow x = y & \text{AIP}
\end{align*}
\]

a constant standing for the unique solution of \( E \) for \( X \) to the constants of BTA. The constant standing for the unique solution of \( E \) for \( X \) is denoted by \( \langle X | E \rangle \). Moreover, we use the following notation. Let \( t \) be a term of BTA and \( E \) be a guarded recursive specification. Then we write \( \langle t | E \rangle \) for \( t \) with, for all \( X \in V(E) \), all occurrences of \( X \) in \( t \) replaced by \( \langle X | E \rangle \). We add the axioms for guarded recursion given in Table 2 to the axioms of BTA. In this table, \( X \), \( t_X \) and \( E \) stand for an arbitrary variable, an arbitrary term of BTA and an arbitrary guarded recursive specification, respectively. Side conditions are added to restrict the variables, terms and guarded recursive specifications for which \( X \), \( t_X \) and \( E \) stand. The additional axioms for guarded recursion are known as the recursive definition principle (RDP) and the recursive specification principle (RSP). The equations \( \langle X | E \rangle = \langle t_X | E \rangle \) for a fixed \( E \) express that the constants \( \langle X | E \rangle \) make up a solution of \( E \). The conditional equations \( E \Rightarrow X = \langle X | E \rangle \) express that this solution is the only one.

We often write \( X \) for \( \langle X | E \rangle \) if \( E \) is clear from the context. It should be borne in mind that, in such cases, we use \( X \) as a constant.

The projective limit characterization of process equivalence on threads is based on the notion of a finite approximation of depth \( n \). When for all \( n \) these approximations are identical for two given threads, both threads are considered identical. This is expressed by the infinitary conditional equation AIP (Approximation Induction Principle) given in Table 3. Following [1, 2], approximation of depth \( n \) is phrased in terms of a unary projection operator \( \pi_n(\cdot) \). The projection operators are defined inductively by means of the axioms P0–P3 given in Table 3. In this table, \( a \) stands for an arbitrary member of \( \mathcal{A}_{\tau u} \). It happens that RSP follows from AIP.

The structural operational semantics of BTA and its extensions with guarded recursion and projection can be found in [5, 4].

Henceforth, we write \( T_{\text{finrec}} \) for the set of all terms of BTA with recursion in which no constants \( \langle X | E \rangle \) for infinite \( E \) occur, and \( T_{\text{finrec}} \) for the set of all closed terms of BTA with recursion in which no constants \( \langle X | E \rangle \) for infinite \( E \) occur. We write \( T_{\text{finrec}}(A) \), where \( A \subseteq \mathcal{A} \), for the set of all closed terms from \( T_{\text{finrec}} \).
that only contain basic actions from $A$. We write $p \in p'$, where $p, p' \in T_{\text{finrec}}$, to indicate that $p$ is a subterm of a term $p'' \in T_{\text{finrec}}$ for which $p' = p''$ is derivable from RDP.

## 4 Interleaving of Threads and Thread Forking

In this section, we extend BTA with an operator for interleaving of threads that supports thread forking.

A thread vector is a sequence of threads. A strategic interleaving operator turns a thread vector of arbitrary length into a single thread. The resulting single thread is sometimes called a multi-thread. Several kinds of strategic interleaving have been elaborated in earlier work, see e.g. [3, 5]. In this section, we only cover one of the simplest interleaving strategies, namely cyclic interleaving with perfect forking.

It is assumed that a fixed but arbitrary thread forking function $\phi: \mathbb{N} \rightarrow T_{\text{finrec}}$, where $\mathbb{N} \subseteq \mathbb{N}$, has been given. Moreover, it is assumed that $nt(n) \in A$ for all $n \in \text{dom}(\phi)$. The basic action $nt(n)$ represents the act of forking off thread $\phi(n)$. We consider the case where forking off a thread will never be blocked or fail. Therefore, it always produces a positive reply. The action $\tau$ arises as the residue of forking off a thread. We write $NT$ for the set $\{nt(n) \mid n \in \text{dom}(\phi)\}$. The strategic interleaving operator for cyclic interleaving with perfect forking is denoted by $\parallel_f(\_)$.

The axioms for cyclic interleaving with perfect forking are given in Table 4.\footnote{We write $\langle \_ \rangle$ for the empty sequence, $(d)$ for the sequence having $d$ as sole element, and $\alpha \bowtie \beta$ for the concatenation of sequences $\alpha$ and $\beta$. We assume that the identities $\alpha \bowtie \langle \_ \rangle = \langle \_ \rangle \bowtie \alpha = \alpha$ hold.}

\begin{table}[h]
\centering
\begin{tabular}{ll}
\hline
$\parallel_f(\langle \_ \rangle) = S$ & CSI1 \\
$\parallel_f(\langle \_ \rangle \bowtie \alpha) = \parallel_f(\alpha)$ & CSI2 \\
$\parallel_f(\langle D \rangle \bowtie \alpha) = S_{D_f}(\parallel_f(\alpha))$ & CSI3 \\
$\parallel_f(\langle x \leq a \bowtie y \rangle \bowtie \alpha) = \parallel_f(\alpha \bowtie \langle x \rangle) \leq a \bowtie \parallel_f(\alpha \bowtie \langle y \rangle)$ & CSI4 \\
$\parallel_f(\langle x \leq nt(n) \bowtie y \rangle \bowtie \alpha) = \tau \bowtie \parallel_f(\alpha \bowtie \langle \phi(n) \rangle \bowtie \langle x \rangle)$ & CSI5 \\
\hline
\end{tabular}
\caption{Axioms for cyclic interleaving with perfect forking}
\end{table}

\begin{table}[h]
\centering
\begin{tabular}{ll}
\hline
$S_{D_f}(S) = D$ & S2D1 \\
$S_{D_f}(D) = D$ & S2D2 \\
$S_{D_f}(x \leq a \bowtie y) = S_{D_f}(x) \leq a \bowtie S_{D_f}(y)$ & S2D3 \\
\hline
\end{tabular}
\caption{Axioms for deadlock at termination}
\end{table}

In CSI3, the auxiliary deadlock at termination operator $S_{D_f}(\_)$ is used. It turns termination into deadlock. Its axioms are given in Table 5. In Table 4, $\alpha$ stands
for an arbitrary member of $A_{\tau} \setminus NT$. In Table 5, $a$ stands for an arbitrary member of $A_{\tau}$. In [3], we treat several strategies for cyclic interleaving with forking. All of them deal with cases where forking may be blocked and/or may fail. We believe that perfect forking is a suitable abstraction when studying the simulation of Turing machines.

The structural operational semantics for cyclic interleaving without forking is given in [5, 4]. The adaptation to the case with perfect forking is obvious.

5 Applying Threads to Maurer Machines

In this section, we introduce Maurer machines and add for each Maurer machine $H$ a binary apply operator $\_ \cdot H \_ \to$ to BTA.

A Maurer machine is a tuple $H = (M, B, S, I, A, [\_])$, where $(M, B, S, I)$ is a Maurer computer and:

- $A \subseteq A \setminus NT$;
- $[\_] : A \rightarrow (I \times M)$.

The members of $A$ are called the basic actions of $H$, and $[\_]$ is called the basic action interpretation function of $H$.

The apply operators associated with Maurer machines are related to the apply operators introduced in [6]. They allow for threads to transform states of the associated Maurer machine by means of its instructions. Such state transformations produce either a state of the associated Maurer machine or the undefined state $\uparrow$. It is assumed that $\uparrow$ is not a state of any Maurer machine. We extend function restriction to $\uparrow$ by stipulating that $\uparrow \rightharpoonup M = \uparrow$ for any set $M$.

The first operand of the apply operator $\_ \cdot H \_ \cdot$ associated with Maurer machine $H = (M, B, S, I, A, [\_])$ must be a term from $T_{\text{finrec}}(A)$ and its second argument must be a state from $S \cup \{\\}$.

Let $H = (M, B, S, I, A, [\_])$ be a Maurer machine, let $p \in T_{\text{finrec}}(A)$, and let $S \in S$. Then $p \cdot H S$ is the state from $S$ that results if all basic actions performed by thread $p$ are processed by the Maurer machine $H$ from initial state $S$. Moreover, let $(I_a, m_a) = [\_]$ for all $a \in A$. Then the processing of a basic action $a$ by $H$ amounts to a state change according to the instruction $I_a$.

In the resulting state, the reply produced by $H$ is contained in memory element $m_a$. If $p$ is $S$, then there will be no state change. If $p$ is $D$, then the result is $\uparrow$.

Let $H = (M, B, S, I, A, [\_])$ be a Maurer machine, and let $(I_a, m_a) = [\_]$ for all $a \in A$. Then the apply operator $\_ \cdot H \_ \cdot$ is defined by the equations given in Table 6 (for $a \in A$ and $S \in S$) and the rule given in Table 7 (for $S \in S$). We say that $p \cdot H S$ is convergent if $\exists n \in \mathbb{N} \cdot \pi_n(p) \cdot H S \neq \uparrow$. If $p \cdot H S$ is convergent, then the length of the computation of $p \cdot H S$, written $|p \cdot H S|$, is the smallest $n \in \mathbb{N}$ such that $\pi_n(p) \cdot H S \neq \uparrow$. If $p \cdot H S$ is not convergent, then $|p \cdot H S|$ is undefined. We say that $p \cdot H S$ is divergent if $p \cdot H S$ is not convergent. Notice that the rule from Table 7 can be read as follows: if $x \cdot H S$ is divergent, then it equals $\uparrow$.  

7
If \((p, S) \in S\)

### 6 Representation of Threads

In this section, we make precise how to represent threads in the memory of a Maurer machine.

It is assumed that a fixed but arbitrary finite set \(M_{thr}\) and a fixed but arbitrary bijection \(m_{thr} : [0, \text{card}(M_{thr}) - 1] \to M_{thr}\) have been given. \(M_{thr}\) is called the thread memory. We write \(\text{size}(M_{thr})\) for \(\text{card}(M_{thr})\). Let \(n, n' \in [0, \text{size}(M_{thr}) - 1]\) be such that \(n \leq n'\). Then, we write \(M_{thr}[n]\) for \(m_{thr}(n)\), and \(M_{thr}[n, n']\) for \(\{m_{thr}(k) \mid n \leq k \leq n'\}\).
The thread memory is a memory of which the elements can be addressed by means of members of \([0, \text{size}(M_{thr}) - 1]\). We write \(A_{thr}\) for \([0, \text{size}(M_{thr}) - 1]\).

The thread memory elements are meant for containing the representations of nodes that form part of a simple graph representation of a thread. Here, the representation of a node is either \(S, D\) or a triple consisting of a basic action and two members of \(A_{thr}\) addressing thread memory elements containing representations of other nodes.

Let \(n, n' \in A_{thr}\) be such that \(n \leq n'\). Then, we write \(B_{thr}[n, n']\) for \([S, D] \cup ([n, n'] \times A \times [n, n'])\). We write \(B_{thr}\) for \(B_{thr}[0, \text{size}(M_{thr}) - 1]\). \(B_{thr}\) is called the thread memory base set. We write \(S_{thr}\) for the set of all functions \(S_{thr}: M_{thr} \rightarrow B_{thr}\).

Let \(p \in T_{finrec}\) be a term not containing \(\tau\). Then the nodes of the graph representation of \(p\), written \(\text{Nodes}(p)\), is the smallest subset of \(T_{finrec}\) such that:

- \(p \in \text{Nodes}(p)\);
- if \(p' \preceq a \succeq p'' \in \text{Nodes}(p)\), then \(p', p'' \in \text{Nodes}(p)\);
- if \(\langle X_0| X_0 = t_0, \ldots, X_n = t_n \rangle \in \text{Nodes}(p)\), \(\langle t_0| X_0 = t_0, \ldots, X_n = t_n \rangle \in \text{Nodes}(p)\).

We write \(\text{size}(p)\) for \(\text{card}(\text{Nodes}(p))\).

It is assumed that for all \(p \in T_{finrec}\), a fixed but arbitrary bijection \(\text{node}_p: [0, \text{size}(p) - 1] \rightarrow \text{Nodes}(p)\) with \(\text{node}_p(0) = p\) has been given.

Let \(p \in T_{finrec}\) be a term not containing \(\tau\), with \(\text{size}(p) \leq \text{size}(M_{thr})\). Then the stored graph representation of \(p\), written \(s_{thr}(p)\), is the unique function \(s_{thr}: M_{thr}[0, \text{size}(p) - 1] \rightarrow B_{thr}[0, \text{size}(p) - 1]\) such that for all \(n \in [0, \text{size}(p) - 1]\), \(s_{thr}(M_{thr}[n]) = \text{repr}_p(\text{node}_p(n))\), where \(\text{repr}_p: \text{Nodes}(p) \rightarrow B_{thr}[0, \text{size}(p) - 1]\) is defined as follows:

\[
\text{repr}_p(S) = S, \\
\text{repr}_p(D) = D, \\
\text{repr}_p(p' \preceq a \succeq p'') = (\text{node}_p^{-1}(p'), a, \text{node}_p^{-1}(p'')), \\
\text{repr}_p(\langle X_0| X_0 = t_0, \ldots, X_n = t_n \rangle) \\
= \text{repr}_p(\langle t_0| X_0 = t_0, \ldots, X_n = t_n \rangle) .
\]

We call \(s_{thr}(p)\) a stored thread.

Notice that \(s_{thr}(p)\) is not defined for \(p\) with \(\text{size}(p) > \text{size}(M_{thr})\). The size of the thread memory restricts the threads that can be stored.

## 7 Turing Machines

Turing machines were proposed almost 70 years ago by Turing in [13]. In this section, we define a kind of Turing machines which is at least as powerful as the kinds of Turing machines that are nowadays often considered as standard (cf. [11, 9]): each Turing machine of those kinds can be simulated by a Turing machine of the kind defined here. The Turing machines of the kind defined here, called simple Turing machines, are closer to the ones proposed by Turing.


First we give an intuitive description of a simple Turing machine. A simple Turing machine consists of a finite-state control, a one-way infinite tape and a tape head. The control can be in any of a finite number of states. The tape is divided into a countably infinite number of cells. Each cell can hold any one of a finite number of tape symbols. One of the tape symbols is the blank symbol $\square$. The tape head is always positioned at one of the tape cells. A simple Turing machine makes steps based on its current state and the tape symbol held in the cell at which the tape head is positioned. In one step it changes state and either overwrites the cell at which the tape head is positioned with some tape symbol or moves the tape head left or right one cell (but not both).

We will fix on $\{0, 1, \square\}$ for the set of tape symbols. We write $B_{tage}$ for the set $\{0, 1, \square\}$. We use the direction symbols $L$ and $R$, and the halt symbol $H$. The symbols $L$, $R$ and $H$ are no tape symbols. We write $D_{hd}$ for the set $\{L, R\}$.

A simple Turing machine $T$ consists of the following components:

- a finite set $Q$;
- a function $\delta : Q \times B_{tage} \rightarrow Q \times (B_{tage} \cup D_{hd} \cup \{H\})$;
- an element $q^0 \in Q$.

The members of $Q$ are called the states, $\delta$ is called the transition function, and $q^0$ is called the initial state.

A contents of the tape of a simple Turing machine is a function $\tau : \mathbb{N} \rightarrow B_{tage}$ for which there exists an $n \in \mathbb{N}$ such that for all $m \in \mathbb{N}$ with $m \geq n$, $\tau(m) = \square$. We write $C_{tage}$ for the set of all such functions.

Let $T = (Q, \delta, q^0)$ be a simple Turing machine. Then a configuration of $T$ is a triple $(q, \tau, i)$, where $q \in Q$, $\tau \in C_{tage}$ and $i \in \mathbb{N}$. If $q = q^0$, then $(q, \tau, i)$ is an initial configuration of $T$. If $\delta(q, \tau(i)) = (q', H)$ for some $q' \in Q$, then $(q, \tau, i)$ is a terminal configuration of $T$. Let $(q, \tau, i)$ and $(q', \tau', i')$ be configurations of $T$. Then $(q', \tau', i')$ is next to $(q, \tau, i)$ in $T$ if for some $s' \in B_{tage} \cup D_{hd}$ such that $s' \neq L$ if $i = 0$:

$$\delta(q, \tau(i)) = (q', s'),$$

for all $j \in \mathbb{N}$:

$$\tau'(j) = s' \quad \text{if } i = j \wedge s' \in B_{tage},$$

$$\tau'(j) = \tau(j) \quad \text{if } i = j \wedge s' \in D_{hd},$$

$$\tau'(j) = \tau(j) \quad \text{if } i \neq j,$$

and

$$i' = i \quad \text{if } s' \in B_{tage},$$

$$i' = i - 1 \quad \text{if } s' = L,$$

$$i' = i + 1 \quad \text{if } s' = R.$$

Let $T = (Q, \delta, q^0)$ be a simple Turing machine. Then the step relation $\vdash_T$ is defined by $(q, \tau, i) \vdash_T (q', \tau', i')$
iff \((q', \tau', i')\) is next to \((q, \tau, i)\) in \(T\). A computation of \(T\) is a finite path
\[\langle (q_0, \tau_0, i_0), \ldots, (q_n, \tau_n, i_n) \rangle\]
in \(\vdash_T\) such that \((q_0, \tau_0, i_0)\) is an initial configuration of \(T\) and \((q_n, \tau_n, i_n)\) is a terminal configuration of \(T\).

In the case of a simple Turing machine, the set of tape symbols is invariably \(B_{tape}\), the tape is a one-way infinite tape, in each step either a tape cell is overwritten or the tape head is moved (but not both), input symbols are not distinguished and accepting states are not distinguished (for the roles of input symbols and accepting states, see e.g. [9]). The definitions given above can easily be adapted to the cases where the set of tape symbols is an arbitrary finite set, the tape is a two-way infinite tape, in each step made both a cell is overwritten and the tape head is moved, input symbols are distinguished and/or accepting states are distinguished. However, it happens that each Turing machine of the kinds resulting from such adaptations can be simulated by a simple Turing machine (for details, see e.g. [8, 7, 11, 9]). Hence, if each simple Turing machine can be simulated on a Maurer machine, then each Turing machine of those other kinds can be simulated on a Maurer machine as well.

\[\text{8 Simulation of Turing Machines}\]

In this section, we show a straightforward way to simulate simple Turing machines on a Maurer machine. Henceforth, simple Turing machines will shortly be called Turing machines.

Assume that a fixed but arbitrary countably infinite set \(M_{tape}\) and a fixed but arbitrary bijection \(m_{tape} : \mathbb{N} \rightarrow M_{tape}\) have been given. \(M_{tape}\) is called a tape memory. Let \(n \in \mathbb{N}\). Then we write \(M_{tape}[n]\) for \(m_{tape}(n)\).

The tape memory is an infinite memory of which the elements can be addressed by means of members of \(\mathbb{N}\). The elements of the tape memory contain 0, 1 or \(\Box\). We write \(S_{tape}\) for the set of all functions \(S_{tape} : M_{tape} \rightarrow B_{tape}\) for which there exists an \(n \in \mathbb{N}\) such that for all \(m \in \mathbb{N}\) with \(m \geq n\), \(S_{tape}(M_{tape}[m]) = \Box\).

The Maurer machines \(TM, TM'\) and \(TM''\) defined in this paper would not be Maurer machines if \(S_{tape}\) was simply the set of all functions \(S_{tape} : M_{tape} \rightarrow B_{tape}\), for Maurer machines may not have states that differ in the contents of infinitely many memory elements.

The memory of the Maurer machine \(TM\) used to simulate Turing machines consists of a tape memory \((M_{tape}\)) a head position register (head) and a reply register (rr). Its instruction set consists of two test instructions (\(I_{test:0}, I_{test:1}\)), two write instructions (\(I_{write:0}, I_{write:1}\)) and two move head instructions (\(I_{mover}, I_{movel}\)). Each instruction is associated with a basic action. The set of basic actions of \(TM\) consists of those basic actions.

It is assumed that \(test:s, write:s \in A\), for all \(s \in B_{tape}\), and \(mover, movel \in A\).

\[\text{5 We interpret the usual remark “no left move is permitted when the read-write head is at the [left] boundary” (see e.g. [11]) as “when the read-write head is at the left boundary, a left move impedes making a step but does not give rise to halting”}\]
$TM$ is the Maurer machine $(M, B, S, I, A, \lfloor \_ \rfloor)$ such that

\[ M = M_{\text{tape}} \cup \{ \text{head}, \text{rr} \}, \]
\[ B = B_{\text{tape}} \cup \mathbb{N} \cup \mathbb{B}, \]
\[ S = \{ S : M \rightarrow B \mid S \in S_{\text{tape}} \land S(\text{head}) \in \mathbb{N} \land S(\text{rr}) \in \mathbb{B} \}, \]
\[ I = \{ \text{test}:s, \text{write}:s \mid s \in B_{\text{tape}} \} \cup \{ \text{mover}, \text{move} \}, \]
\[ A = \{ \text{test}:s, \text{write}:s \mid s \in B_{\text{tape}} \} \cup \{ \text{mover}, \text{move} \}, \]
\[ [a] = (I_a, \text{rr}) \quad \text{for all } a \in A. \]

Here, for each $s \in B_{\text{tape}}$, $I_{\text{test}:s}$ is the unique function from $S$ to $S$ such that for all $S \in S$:

\[
\begin{align*}
I_{\text{test}:s}(S) | M_{\text{tape}} &= S | M_{\text{tape}}, \\
I_{\text{test}:s}(S)(\text{head}) &= S(\text{head}), \\
I_{\text{test}:s}(S)(\text{rr}) &= T \quad \text{if } S(M_{\text{tape}}[S(\text{head})]) = s, \\
I_{\text{test}:s}(S)(\text{rr}) &= F \quad \text{if } S(M_{\text{tape}}[S(\text{head})]) \neq s.
\end{align*}
\]

for each $s \in B_{\text{tape}}$, $I_{\text{write}:s}$ is the unique function from $S$ to $S$ such that for all $S \in S$ and $n \in \mathbb{N}$:

\[
\begin{align*}
I_{\text{write}:s}(S)(M_{\text{tape}}[S(\text{head})]) &= s, \\
I_{\text{write}:s}(S)(M_{\text{tape}}[n]) &= S(M_{\text{tape}}[n]) \quad \text{if } S(\text{head}) \neq n, \\
I_{\text{write}:s}(S)(\text{head}) &= S(\text{head}), \\
I_{\text{write}:s}(S)(\text{rr}) &= T; \\
I_{\text{move}} &\text{ is the unique function from } S \text{ to } S \text{ such that for all } S \in S: \\
I_{\text{move}}(S) | M_{\text{tape}} &= S | M_{\text{tape}}, \\
I_{\text{move}}(S)(\text{head}) &= S(\text{head}) + 1, \\
I_{\text{move}}(S)(\text{rr}) &= T; \\
I_{\text{move}} &\text{ is the unique function from } S \text{ to } S \text{ such that for all } S \in S:
\end{align*}
\]

\[
\begin{align*}
I_{\text{move}}(S) | M_{\text{tape}} &= S | M_{\text{tape}}, \\
I_{\text{move}}(S)(\text{head}) &= S(\text{head}) - 1 \quad \text{if } S(\text{head}) > 0, \\
I_{\text{move}}(S)(\text{head}) &= 0 \quad \text{if } S(\text{head}) = 0, \\
I_{\text{move}}(S)(\text{rr}) &= T \quad \text{if } S(\text{head}) > 0, \\
I_{\text{move}}(S)(\text{rr}) &= F \quad \text{if } S(\text{head}) = 0.
\end{align*}
\]

We write $S_{TM}$ and $A_{TM}$ for the set of states of $TM$ and the set of basic actions of $TM$, respectively.

A Turing thread is a constant $(X_0)\{X_0 = t_0, \ldots, X_n = t_n\} \in T_{\text{finrec}}$, where $t_0, \ldots, t_n$ are terms of the form $t \leq \text{test}: \exists t' \leq \text{test}: 1 \geq t''$ with $t$, $t'$ and $t''$ of the form \text{write}:X\circ X, \text{mover}\circ X, X \leq \text{move} \circ D$ or $S$ ($s \in B_{\text{tape}}, X \in \{X_0, \ldots, X_n\}$).

Each Turing machine can be simulated on the Maurer machine $TM$ by means of a Turing thread $p \in T_{\text{finrec}}(A_{TM})$. 

12
Theorem 1. Let $T = (Q, \delta, q^0)$ be a Turing machine. Then there exists a Turing thread $p \in T_{\text{finrec}}(A_{TM})$ such that for all computations $c$ of $T$, there exists an $S \in S_{TM}$ such that the computation of $p \cdot TM \cdot S$ simulates $c$.

Proof. Suppose that $Q = \{q_0, \ldots, q_n\}$. Let $E$ be the guarded recursive specification $\{X_i = t_{i0} \leq \text{test}:0 \geq (t_{i1} \leq \text{test}:1 \geq t_{i0}) \mid 0 \leq i \leq n\}$, where

\begin{align*}
t_{i0} &= \text{write:} s' \circ X_j \quad \text{if } \delta(q_i, s) = (q_j, s') \land s' \in B_{\text{tape}}; \\
t_{i1} &= \text{mover} \circ X_j \quad \text{if } \delta(q_i, s) = (q_j, R) \\
t_{is} &= X_j \leq \text{movel} \geq D \quad \text{if } \delta(q_i, s) = (q_j, L) \\
t_{is} &= S \quad \text{if } \exists q \in Q \cdot \delta(q_i, s) = (q, H).
\end{align*}

Define $\phi : Q \to T_{\text{finrec}}(A_{TM})$ by $\phi(q_i) = \langle X_i | E \rangle$ ($0 \leq i \leq n$). Clearly, $\phi(q_i)$ is a Turing thread. Define $\phi' : C_{\text{tape}} \times N \to S_{TM}$ by $\phi'(\tau, i)$ is the unique state $S \in S_{TM}$ such that $S(M_{\text{tape}[j]}) = \tau(j)$ for all $j \in N$, $S(\text{head}) = i$ and $S(\text{tr}) = T$. Combine $\phi$ and $\phi'$ to $\phi^* : Q \times C_{\text{tape}} \times N \to T_{\text{finrec}}(A_{TM}) \times S_{TM}$ defined by $\phi^*(q, \tau, i) = (\phi(q), \phi'(\tau, i))$. Then we have $(q, \tau, i) \vdash_{TM} (q', \tau', i')$ iff $\phi^*(q, \tau, i) \vdash_{TM} \phi^*(q', \tau', i')$. This is easily proved by distinction between the following cases: $\delta(q, \tau(i)) \in Q \times B_{\text{tape}}, \delta(q, \tau(i)) \in Q \times \{R\}, \delta(q, \tau(i)) \in Q \times \{L\}, \delta(q, \tau(i)) \in Q \times \{H\}$. It follows immediately that, if $c = \langle (q_0, \tau_0, i_0), \ldots, (q_n, \tau_n, i_n) \rangle$ is a computation of $T$, the computation of $\phi(q_0) \cdot TM \cdot \phi^*(\tau_0, i_0)$ simulates $c$. \hfill \Box

Looking at the instructions used in the simulation of Turing machines on the Maurer machine $TM$, we observe that the test instructions $I_{\text{test},s}$ have an infinite input region and a finite output region and that the write instructions $I_{\text{write},s}$ have a finite input region and an infinite output region. It is easy to see that these infinite regions are essential for many Turing machines. For example, consider the Turing machine that, starting from head position 0, overwrites cells that hold 0 with 1 and cells that hold 1 with 0 and halts when the first cell holding \square is reached. Infinite input and output regions are essential for this Turing machine because the first cell holding \square may occur anywhere on the tape and the Turing machine has only a finite-state control. However, if we expand Turing threads to threads definable by infinite recursive specifications, we can simulate all Turing machines using test and write instructions with a finite input region and a finite output region.

9 Using Instructions with Finite Input & Output Regions

In order to simulate Turing machines using test and write instructions with a finite input region and a finite output region, we have to adapt the Maurer machine $TM$. Moreover, for each Turing machine, we have to adapt the corresponding Turing thread. It happens that the Turing threads can be adapted in a uniform way.

We adapt the Maurer machine $TM$ by removing the head position register $\text{head}$ from the memory and the move head instructions $I_{\text{movel}}$ and $I_{\text{movr}}$ from the instruction set. In addition, we replace each test instruction $I_{\text{test},s}$ by a test
inductively defined as follows: We write \( X \) of a term \( i \in \{ H, P \} \) for all \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \). Each instruction is associated with a basic action. We replace the basic actions of \( TM \) by those basic actions.

It is assumed that \( \text{test}: s:n, \text{write}: s:n \in A \) for all \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \).

\( TM' \) is the Maurer machine \((M, B, S, I, A, \{\_\})\) such that

\[
\begin{align*}
M &= M_{\text{tape}} \cup \{ \tau \}, \\
B &= B_{\text{tape}} \cup B, \\
S &= \{ S : M \to B \mid S | M_{\text{tape}} \in S_{\text{tape}} \land S(\tau) \in B \}, \\
I &= \{ \text{test}: s:n, \text{write}: s:n \mid s \in B_{\text{tape}} \land n \in \mathbb{N} \}, \\
A &= \{ \text{test}: s:n, \text{write}: s:n \mid s \in B_{\text{tape}} \land n \in \mathbb{N} \}, \\
[a] &= (I_s, \tau) \quad \text{for all } a \in A.
\end{align*}
\]

Here, for each \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \), \( I_{\text{test}: s:n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
\begin{align*}
I_{\text{test}: s:n}(S) | M_{\text{tape}} &= S | M_{\text{tape}}, \\
I_{\text{test}: s:n}(S)(\tau) &= \text{T} \quad \text{if } S(M_{\text{tape}}[n]) = s, \\
I_{\text{test}: s:n}(S)(\tau) &= \text{F} \quad \text{if } S(M_{\text{tape}}[n]) \neq s;
\end{align*}
\]

for each \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \), \( I_{\text{write}: s:n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \) and \( m \in \mathbb{N} \):

\[
\begin{align*}
I_{\text{write}: s:n}(S)(M_{\text{tape}}[n]) &= s, \\
I_{\text{write}: s:n}(S)(M_{\text{tape}}[m]) &= S(M_{\text{tape}}[m]) \quad \text{if } n \neq m, \\
I_{\text{write}: s:n}(S)(\tau) &= \text{T}.
\end{align*}
\]

We write \( S_{TM'} \) and \( A_{TM'} \) for the set of states of \( TM' \) and the set of basic actions of \( TM' \), respectively.

Let \( (X_0[E], E = \{ X_0 = t_0, \ldots, X_n = t_n \} \), be a Turing thread, let \( i \in \{ 0, \ldots, n \} \), and let \( k \in \mathbb{N} \). Moreover, let \( T_0 \) be the set of all subterms of a term \( t \in T_{\text{finrec}} \) for which \( t_0 = t \) is derivable from \( E \). Then the relation \( \mathcal{HP}_{X_i} \subseteq T_0 \times \mathbb{N} \) is inductively defined as follows:

- if \( X_i \in T_0 \), then \( \mathcal{HP}_{X_i}(X_i, 0) \);
- if \( \mathcal{HP}_{X_i}(t, l), t \leq \text{test}: s \geq t' \in T_0 \) and \( l \geq 0 \), then \( \mathcal{HP}_{X_i}(t \leq \text{test}: s \geq t', l) \);
- if \( \mathcal{HP}_{X_i}(t, l), t' \leq \text{test}: s \geq t \in T_0 \) and \( l \geq 0 \), then \( \mathcal{HP}_{X_i}(t' \leq \text{test}: s \geq t, l) \);
- if \( \mathcal{HP}_{X_i}(t, l), \text{write}: s \circ t \in T_0 \) and \( l \geq 0 \), then \( \mathcal{HP}_{X_i}(\text{write}: s \circ t, l) \);
- if \( \mathcal{HP}_{X_i}(t, l), \text{move}: t \in T_0 \) and \( l \geq 0 \), then \( \mathcal{HP}_{X_i}(\text{move}: t, l + 1) \);
- if \( \mathcal{HP}_{X_i}(t, l), l \leq \text{movel} \geq D \in T_0 \) and \( l \geq 0 \), then \( \mathcal{HP}_{X_i}(l \leq \text{movel} \geq D, l - 1) \).

We write \( X_0 \xrightarrow{k} E X_i \) to indicate that there exist a \( t \in T_{\text{finrec}} \) such that \( t_0 = t \) is derivable from \( E \) and \( \mathcal{HP}_{X_i}(t, k) \) holds. The recursive specification \( \psi(E) \) is inductively defined as follows:

- if \( X_0 \xrightarrow{k} E X_i \), then \( X_{ik} = t_{ik} \in \psi(E) \),
  where \( t_{ik} \) is obtained from \( t_i \) by applying the following replacement rules:
• test: is replaced by test: k;
• write: o Xj is replaced by write: k o Xj;
• mover o Xj is replaced by Xj, where l = k + 1;
• if k ≠ 0, then Xj ≤ mover ≥ D is replaced by Xj, where l = k - 1;
• if k = 0, then Xj ≤ mover ≥ D is replaced by D.

We write ψ((X₀|ψ)) for (X₀|ψ(E)).

The variables of a Turing thread p correspond to the states of a Turing machine. If the head position is made part of the instructions, a different copy of a state is needed for each different head position that may occur when the Turing machine enters that state. The variables of ψ(p) correspond to those new states. Consequently, applying Turing thread p to Maurer machine TM from some state of TM has the same effect as applying ψ(p) to Maurer machine TM′ from the corresponding state of TM′.

**Theorem 2.** Let p be a Turing thread, and let S₀ ∈ S_TM and S₀′ ∈ S_TM be such that S₀ | (Mtape ∪ {r}) = S₀ and S₀(head) = 0. Then (p ⋄ TM S₀) | (Mtape ∪ {r}) = ψ(p) ⋄ TM′ S₀′.

Proof. It is easy to see that for all S ∈ S_TM:

\[ I_{test}.s(S) \upharpoonright (Mtape \cup \{r\}) = I_{test}.s.n(S \upharpoonright (Mtape \cup \{r\})) \]

\[ I_{write}.s(S) \upharpoonright (Mtape \cup \{r\}) = I_{write}.s.n(S \upharpoonright (Mtape \cup \{r\})) \]

\[ I_{mover}(S) \upharpoonright Mtape = S \upharpoonright Mtape \]

\[ I_{movel}(S) \upharpoonright Mtape = S \upharpoonright Mtape \]

where n = S(head).

Let (pₙ, Sₙ) be the n+1-th element in the full path of p ⋄ TM S₀ of which the first component equals S, D or q ≤ test: 0 ≥ r for some q, r ∈ T finrec, and let (pₙ′, Sₙ′) be the n+1-th element in the full path of ψ(p) ⋄ TM′ (S₀ | (Mtape ∪ {r})) of which the first component equals S, D or q′ ≤ test: 0 ≥ r′ for some k ∈ N and q′, r′ ∈ T finrec. Then, using the above equations, it is straightforward to prove by induction on n that:

- \( pₙ = q ≤ test: 0 ≥ r \) and \( Sₙ(head) = k \) if \( pₙ′ = q′ ≤ test: 0 ≥ r′ \) with \( q′ \) and \( r′ \) obtained from \( q \) and \( r \) by applying the replacement rules given in the definition of ψ above;
- \( Sₙ | (Mtape \cup \{r\}) = Sₙ′ \)

(for n < |p ⋄ TM S₀| if p ⋄ TM S₀ is convergent). From this, the theorem follows immediately. □

Theorem 2 deals only with the case where the initial head position is 0. This is sufficient to conclude that each Turing machine can be simulated on the Maurer machine TM′ by means of an adapted Turing thread, for each Turing machine can be simulated by a (simple) Turing machine of which the initial head position is restricted to 0.
Consider again the Turing machine that, starting from head position 0, overwrites cells that hold 0 with 1 and cells that hold 1 with 0 and halts when the first cell holding □ is reached. The Turing thread that corresponds to the finite-state control of this Turing machine is the constant \( \langle X_0 | E \rangle \), where

\[
E = \{ X_0 = \text{write}:1 \circ X_1 \triangleleft \text{test}:0 \triangleright (\text{write}:0 \circ X_1 \triangleleft \text{test}:1 \triangleright S), \\
X_1 = \text{mover} \circ X_0 \triangleleft \text{test}:0 \triangleright (\text{mover} \circ X_0 \triangleleft \text{test}:1 \triangleright \text{mover} \circ X_0) \}.
\]

Clearly, \( X_0 \xrightarrow{k, E} X_0 \) for each \( k \in \mathbb{N} \). Consequently, in this case \( \psi(E) \) is an infinite-state thread. We will show in Section 10 that, when simulating Turing machines on a Maurer machine using test and write instructions with a finite input region and a finite output region, we can get around infinite-state threads in the case of convergent computations.

Hitherto, the results concerning the simulation of Turing machines are closely related to well-known facts about Turing machines. In Maurer’s terminology, the facts concerned can be phrased as follows:

- the instruction implicitly executed by a Turing machine on a test step has an infinite input region and a finite output region;
- the instruction implicitly executed by a Turing machine on a write step has a finite input region and an infinite output region;
- these instructions can be replaced by instructions with a finite input region and a finite output region if we allow Turing machines with an infinite set of states.

10 Using a Multi-thread and Thread Forking

In this section, we show a way to simulate Turing machines on a Maurer machine using test and write instructions with a finite input region and a finite output region that gets around infinite-state threads in the case of convergent computations. The basic ideas behind it are as follows:

- the thread corresponding to the finite-state control of the Turing machine in question is stored and then executed under control of a multi-thread that makes the head position part of the instructions;
- this multi-thread forks off for every head position a control thread of itself on the head reaching the preceding position for the first time.

By using thread forking in this way, the execution remains controlled by a finite thread if the computation concerned is convergent. Although it is not necessary to get around infinite-state threads, the head position register \( \text{head} \) will be replaced by a countably infinite memory.

It is assumed that a fixed but arbitrary countably infinite set \( M_{hd} \) and a fixed but arbitrary bijection \( m_{hd} : \mathbb{N} \rightarrow M_{hd} \) have been given. \( M_{hd} \) is called a \( \text{head position memory} \). Let \( n \in \mathbb{N} \). Then we write \( M_{hd}[n] \) for \( m_{hd}(n) \). \( M_{hd} \) is an infinite memory of which the elements can be addressed by means of members of
The elements of $M_{\text{hd}}$ contain $T$ or $F$. We write $S_{\text{hd}}$ for the set of all functions $S_{\text{hd}} : M_{\text{hd}} \to \mathbb{B}$ for which there exists an $n \in \mathbb{N}$ such that $S_{\text{hd}}(M_{\text{hd}}[n]) = T$ and for all $m \in \mathbb{N}$ with $m \neq n$, $S_{\text{hd}}(M_{\text{hd}}[m]) = F$. $M_{\text{hd}}$ will be used in such a way that the head position is always the unique $n$ for which $M_{\text{hd}}[n]$ contains $T$. The memory of the simulating Maurer machine remains countably infinite if head is replaced by $M_{\text{hd}}$. The replacement achieves that, for each memory element, all possible contents belong to a finite set.

The Maurer machine $TM''$ defined below would not be a Maurer machine if $S_{\text{hd}}$ was simply the set of all functions $S_{\text{hd}} : M_{\text{hd}} \to \mathbb{B}$, for Maurer machines may not have states that differ in the contents of infinitely many memory elements.

We adapt the Maurer machine $TM$ by extending the memory with a thread memory ($M_{\text{thr}}$), a thread location register ($\text{tlr}$) and a basic action register ($\text{bar}$), and the instruction set with a halt instruction ($I_{\text{halt}}$), a fetch instruction ($I_{\text{fetch}}$), an execute stored basic action instruction ($I_{\text{exsba}}$) for each $n \in \mathbb{N}$, an test execution mode instruction ($I_{\text{testem}}$), and a test head position instruction ($I_{\text{testhp}}$) for each $n \in \mathbb{N}$. Each of these extra instructions is associated with a basic action. We replace the basic actions of $TM$ by those basic actions. In addition, we replace the head position register head by a head position memory $M_{\text{hd}}$, each test instruction $I_{\text{test}}$ by a test instruction $I_{\text{test},s}$ for each $n \in \mathbb{N}$, and each write instruction $I_{\text{write},s}$ by a write instruction $I_{\text{write},s}$ for each $n \in \mathbb{N}$.

The thread memory $M_{\text{thr}}$ is meant for storing a Turing thread $p$. Processing of a basic action performed by $p$ now amounts to first fetching the basic action from $M_{\text{thr}}$, in the basic action register $\text{bar}$ and then executing the basic action in $\text{bar}$. The thread location register $\text{tlr}$ is meant for containing the address of the thread memory element from which most recently a basic action has been fetched. The contents of that thread memory element, together with the reply produced at completion of the execution of the basic action concerned, determines the thread memory element from which next time a basic action must be fetched. To indicate that no basic action has been fetched yet, the $\text{tlr}$ must initially contain $-1$. The thread memory element from which the first time a basic action must be fetched is the one at address $0$. The instruction $I_{\text{exsba}}$ allows for making the head position part of the instruction that corresponds to the basic action in $\text{bar}$. The instruction $I_{\text{testhp}}$ is meant for testing whether the head position is $n$. The instruction $I_{\text{testem}}$ allows for testing whether the execution of the stored Turing thread has not yet come to an end.

Once again, it is assumed that $\text{test}:s,\text{write}:s \in A$, for all $s \in B_{\text{tape}}$, and $\text{mover},\text{movel} \in A$. Moreover, it is assumed that $\text{testem},\text{halt},\text{fetch} \in A$ and $\text{testhp},\text{exsba} \in A$ for all $n \in \mathbb{N}$.

$TM''$ is the Maurer machine $(M,B,S,I,A,[\_])$ such that

\[
M = M_{\text{tape}} \cup M_{\text{hd}} \cup M_{\text{thr}} \cup \{\text{tlr, bar, rr}\}, \\
B = B_{\text{tape}} \cup \mathbb{B} \cup B_{\text{thr}} \cup A_{\text{thr}} \cup \{-1\} \cup A_{TM}, \\
S = \{S : M \to B | \\
S(\text{tlr}) \in A_{\text{thr}} \cup \{-1\} \land S(\text{bar}) \in A_{TM} \land S(\text{rr}) \in \mathbb{B} \} ,
\]
\[ I = \{ I_{\text{test}:s,n}, I_{\text{write}:s,n} \mid s \in B_{\text{tape}} \land n \in \mathbb{N} \} \cup \{ I_{\text{mover}}, I_{\text{mover}} \} \]
\[ \cup \{ I_{\text{testem}, I_{\text{halt}}, I_{\text{fetch}}} \} \cup \{ I_{\text{testhp:n}, I_{\text{exsb}:n}} \mid n \in \mathbb{N} \}, \]
\[ A = \{ \text{testem, halt, fetch} \} \cup \{ \text{testhp:n, exsb:n} \mid n \in \mathbb{N} \}, \]
\[ [a] = (I_a, r) \quad \text{for all } a \in A. \]

Here, \( I_{\text{testem}} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{testem}}(S) \mid M_{\text{tape}} = S \mid M_{\text{tape}},
\]
\[
I_{\text{testem}}(S) \mid M_{\text{hd}} = S \mid M_{\text{hd}},
\]
\[
I_{\text{testem}}(S) \mid M_{\text{thr}} = S \mid M_{\text{thr}},
\]
\[
I_{\text{testem}}(S)(\text{thr}) = S(\text{thr}),
\]
\[
I_{\text{testem}}(S)(\text{bar}) = S(\text{bar}),
\]
\[
I_{\text{testem}}(S)(\text{rr}) = \begin{cases} T & \text{if } S(M_{\text{thr}}[S(\text{thr})]) \in \{ S, D \}, \\ F & \text{if } S(M_{\text{thr}}[S(\text{thr})]) \notin \{ S, D \}; \end{cases}
\]

\( I_{\text{halt}} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{halt}}(S) \mid M_{\text{tape}} = S \mid M_{\text{tape}},
\]
\[
I_{\text{halt}}(S) \mid M_{\text{hd}} = S \mid M_{\text{hd}},
\]
\[
I_{\text{halt}}(S) \mid M_{\text{thr}} = S \mid M_{\text{thr}},
\]
\[
I_{\text{halt}}(S)(\text{thr}) = S(\text{thr}),
\]
\[
I_{\text{halt}}(S)(\text{bar}) = S(\text{bar}),
\]
\[
I_{\text{halt}}(S)(\text{rr}) = \begin{cases} T & \text{if } S(M_{\text{thr}}[S(\text{thr})]) = S, \\ F & \text{if } S(M_{\text{thr}}[S(\text{thr})]) \neq S; \end{cases}
\]

\( I_{\text{fetch}} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{fetch}}(S) \mid M_{\text{tape}} = S \mid M_{\text{tape}},
\]
\[
I_{\text{fetch}}(S) \mid M_{\text{hd}} = S \mid M_{\text{hd}},
\]
\[
I_{\text{fetch}}(S) \mid M_{\text{thr}} = S \mid M_{\text{thr}},
\]
\[
I_{\text{fetch}}(S)(\text{thr}) = ntl(S, r),
\]
\[
I_{\text{fetch}}(S)(\text{bar}) = \begin{cases} \pi_2(S(M_{\text{thr}}[\text{ntl}(S, r)])) & \text{if } S(M_{\text{thr}}[\text{ntl}(S, r)]) \notin \{ S, D \}, \\ S(\text{bar}) & \text{if } S(M_{\text{thr}}[\text{ntl}(S, r)]) \in \{ S, D \}, \end{cases}
\]
\[
I_{\text{fetch}}(S)(\text{rr}) = \begin{cases} T & \text{if } S(M_{\text{thr}}[\text{ntl}(S, r)]) \notin \{ S, D \}, \\ F & \text{if } S(M_{\text{thr}}[\text{ntl}(S, r)]) \in \{ S, D \}; \end{cases}
\]

where \( r = S(\text{rr}) \) and \( ntl : S \times B \to A_{\text{thr}} \) is defined as follows:

\[
ntl(S, T) = \begin{cases} \pi_1(S(M_{\text{thr}}[S(\text{thr})])) & \text{if } S(\text{thr}) \in A_{\text{thr}} \land S(M_{\text{thr}}[S(\text{thr})]) \notin \{ S, D \}, \\ ntl(S, F) = \begin{cases} \pi_3(S(M_{\text{thr}}[S(\text{thr})])) & \text{if } S(\text{thr}) \in A_{\text{thr}} \land S(M_{\text{thr}}[S(\text{thr})]) \notin \{ S, D \}, \\ ntl(S, r') = S(\text{thr}) & \text{if } S(\text{thr}) \in A_{\text{thr}} \land S(M_{\text{thr}}[S(\text{thr})]) \in \{ S, D \}, \\ ntl(S, r') = 0 & \text{if } S(\text{thr}) \notin A_{\text{thr}}; \end{cases} \end{cases}
\]
for each \( n \in \mathbb{N} \), \( I_{\text{test}: s, n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{test}: s, n}(S) \upharpoonright \text{tape} = S \upharpoonright \text{tape},
I_{\text{test}: s, n}(S) \upharpoonright \text{hd} = S \upharpoonright \text{hd},
I_{\text{test}: s, n}(S) \upharpoonright \text{thr} = S \upharpoonright \text{thr},
I_{\text{test}: s, n}(S)(\text{tlr}) = S(\text{tlr}),
I_{\text{test}: s, n}(S)(\text{bar}) = S(\text{bar}),
I_{\text{test}: s, n}(S)(\text{rr}) = S(S_{\text{hd}[n]});
\]

for each \( n \in \mathbb{N} \), \( I_{\text{exsba}: n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{exsba}: n}(S) = tmi(S(\text{bar}), n)(S),
\]

where \( tmi : A_{\text{TM}} \times \mathbb{N} \to I \) is defined as follows:

\[
tmi(\text{test}, s, n) = I_{\text{test}, s, n},
I_{\text{write}, s, n} = I_{\text{write}, s, n},
I_{\text{mov}, n} = I_{\text{mov}, n},
\]

for each \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \), \( I_{\text{test}: s, n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \):

\[
I_{\text{test}: s, n}(S) \upharpoonright \text{tape} = S \upharpoonright \text{tape},
I_{\text{test}: s, n}(S) \upharpoonright \text{hd} = S \upharpoonright \text{hd},
I_{\text{test}: s, n}(S) \upharpoonright \text{thr} = S \upharpoonright \text{thr},
I_{\text{test}: s, n}(S)(\text{tlr}) = S(\text{tlr}),
I_{\text{test}: s, n}(S)(\text{bar}) = S(\text{bar}),
I_{\text{test}: s, n}(S)(\text{rr}) = \text{T} \quad \text{if} \ S(S_{\text{tape}[n]}) = s,
I_{\text{test}: s, n}(S)(\text{rr}) = \text{F} \quad \text{if} \ S(S_{\text{tape}[n]}) \neq s;
\]

for each \( s \in B_{\text{tape}} \) and \( n \in \mathbb{N} \), \( I_{\text{write}: s, n} \) is the unique function from \( S \) to \( S \) such that for all \( S \in S \) and \( m \in \mathbb{N} \):

\[
I_{\text{write}: s, n}(S)(S_{\text{tape}[n]}) = s,
I_{\text{write}: s, n}(S)(S_{\text{tape}[m]}) = S(S_{\text{tape}[m]}) \quad \text{if} \ n \neq m,
I_{\text{write}: s, n}(S) \upharpoonright \text{hd} = S \upharpoonright \text{hd},
I_{\text{write}: s, n}(S) \upharpoonright \text{thr} = S \upharpoonright \text{thr},
I_{\text{write}: s, n}(S)(\text{tlr}) = S(\text{tlr}),
I_{\text{write}: s, n}(S)(\text{bar}) = S(\text{bar}),
I_{\text{write}: s, n}(S)(\text{rr}) = \text{T};
\]
Theorem 3. Let $p$ be a Turing thread such that $\text{size}(p) \leq \text{size}(\text{M}_{\text{th}})$, and let $S_0 \in S_{TM}$ and $S_0'' \in S_{TM''}$ be such that $S_0 \upharpoonright (\text{M}_{\text{tape}} \cup \{\text{tr}\}) = S_0'' \upharpoonright (\text{M}_{\text{tape}} \cup \{\text{tr}\})$,

$I_{\text{mover}}$ is the unique function from $S$ to $S$ such that for all $S \in S$:

\[
I_{\text{mover}}(S) \upharpoonright \text{M}_{\text{tape}} = S \upharpoonright \text{M}_{\text{tape}},
\]

\[
I_{\text{mover}}(S) \upharpoonright \text{M}_{\text{hd}} = \text{shift}(S \upharpoonright \text{M}_{\text{hd}}),
\]

\[
I_{\text{mover}}(S) \upharpoonright \text{M}_{\text{thr}} = S \upharpoonright \text{M}_{\text{thr}},
\]

\[
I_{\text{mover}}(S)(\text{thr}) = S(\text{thr}),
\]

\[
I_{\text{mover}}(S)(\text{bar}) = S(\text{bar}),
\]

\[
I_{\text{mover}}(S)(\text{tr}) = T, \]

where $\text{shift} : S_{\text{hd}} \to S_{\text{hd}}$ is defined as follows ($n \in \mathbb{N}$):

\[
\text{shift}(S)(\text{M}_{\text{hd}}[0]) = F, \]

\[
\text{shift}(S)(\text{M}_{\text{hd}}[n + 1]) = S(\text{M}_{\text{hd}}[n]).
\]

and, $I_{\text{mvel}}$ is the unique function from $S$ to $S$ such that for all $S \in S$:

\[
I_{\text{mvel}}(S) \upharpoonright \text{M}_{\text{tape}} = S \upharpoonright \text{M}_{\text{tape}},
\]

\[
I_{\text{mvel}}(S) \upharpoonright \text{M}_{\text{hd}} = \text{shift}(S \upharpoonright \text{M}_{\text{hd}}),
\]

\[
I_{\text{mvel}}(S) \upharpoonright \text{M}_{\text{thr}} = S \upharpoonright \text{M}_{\text{thr}},
\]

\[
I_{\text{mvel}}(S)(\text{thr}) = S(\text{thr}),
\]

\[
I_{\text{mvel}}(S)(\text{bar}) = S(\text{bar}),
\]

\[
I_{\text{mvel}}(S)(\text{tr}) = \neg S(\text{M}_{\text{hd}}[0]),
\]

where $\text{shift} : S_{\text{hd}} \to S_{\text{hd}}$ is defined as follows ($n \in \mathbb{N}$):

\[
\text{shift}(S)(\text{M}_{\text{hd}}[0]) = T \text{ if } S(\text{M}_{\text{hd}}[0]) = T,
\]

\[
\text{shift}(S)(\text{M}_{\text{hd}}[0]) = S(\text{M}_{\text{hd}}[1]) \text{ if } S(\text{M}_{\text{hd}}[0]) = F,
\]

\[
\text{shift}(S)(\text{M}_{\text{hd}}[n + 1]) = S(\text{M}_{\text{hd}}[n + 2]).
\]

Let $n \in \mathbb{N}$, and let $CE_n$ be the guarded recursive specification over BTA that consists of the following equations:

\[
CT_n = (n(t(n + 1) \circ CT'_n) \leq \text{testhp} : n \geq (CT_n \leq \text{testem} \geq S),
\]

\[
CT'_n = (\text{exsh} : n \circ CT''_n) \leq \text{fetch} \geq (S \leq \text{halt} \geq D),
\]

\[
CT''_n = CT'_n \leq \text{testhp} : n \geq (CT''_n \leq \text{testem} \geq S).
\]

Moreover, take the function $\phi$ from $\mathbb{N}$ to $\mathcal{T}_{\text{finrec}}$ defined by $\phi(n) = (CT_n | CE_n)$ as the thread forking function. Then applying Turing thread $p$ to the Maurer machine $TM$ from some state of $TM$ in which the head position is 0 has the same effect as applying $||_t((CT_0))$ to the Maurer machine $TM''$ from the corresponding state of $TM''$ in which the thread memory contains the stored graph representation of $p$.

Theorem 3. Let $p$ be a Turing thread such that size($p$) $\leq$ size($\text{M}_{\text{th}}$), and let $S_0 \in S_{TM}$ and $S_0'' \in S_{TM''}$ be such that $S_0 \upharpoonright (\text{M}_{\text{tape}} \cup \{\text{tr}\}) = S_0'' \upharpoonright (\text{M}_{\text{tape}} \cup \{\text{tr}\})$. 

20
Proof. It is easy to see that for all $S \in S_{TM}$, $S'' \in S_{TM''}$ and $n, n' \in \mathbb{N}$ such that $S \mid (M_{tape} \cup \{rr\}) = S'' \mid (M_{tape} \cup \{rr\})$, $S(\text{head}) = n$ and $S''(\text{Mhd}[n]) = T$:

$$I_{\text{test.s}}(S) \mid (M_{tape} \cup \{rr\}) = I_{\text{test.s,n}}(S'') \mid (M_{tape} \cup \{rr\}),$$
$$I_{\text{write.s}}(S) \mid (M_{tape} \cup \{rr\}) = I_{\text{write.s,n}}(S'') \mid (M_{tape} \cup \{rr\}),$$
$$I_{\text{move.s}}(S) \mid (M_{tape} \cup \{rr\}) = I_{\text{move.s}}(S'') \mid (M_{tape} \cup \{rr\}),$$
$$I_{\text{move.s}}(S) \mid (M_{tape} \cup \{rr\}) = I_{\text{move.s}}(S'') \mid (M_{tape} \cup \{rr\}),$$

$$I_{\text{test.s}}(S)(\text{head}) = n' \iff I_{\text{test.s,n}}(S''(\text{Mhd}[n'])) = T,$$
$$I_{\text{write.s}}(S)(\text{head}) = n' \iff I_{\text{write.s,n}}(S''(\text{Mhd}[n'])) = T,$$
$$I_{\text{move.s}}(S)(\text{head}) = n' \iff I_{\text{move.s}}(S''(\text{Mhd}[n'])) = T,$$
$$I_{\text{move.s}}(S)(\text{head}) = n' \iff I_{\text{move.s}}(S''(\text{Mhd}[n'])) = T.$$

Let $(\|i\|_{\text{ct}(0)}(\text{Mhd}[0]), S''')_{\text{TM}''} \overset{+}{\rightarrow} (\|i\|_{\text{ct}(1)} \ldots \overset{\sim}{\vdash} (p_1))$, $S'')$. Then we have for all $i, j \in [1, l]$, $n \in \mathbb{N}$ and $s \in B_{\text{tape}}$:

1. (a) if $p_i \in CT_n$ and $p_j \in CT_n$, then $i = j$,
   (b) if $n(n + 1) \circ CT_n \in p_i \iff n = \max\{m \mid \exists k \in [1, l] \bullet p_k \in CT_m\};$
2. if $S''(\text{Mhd}[n]) = T$, then:
   (a) there exists a unique $k \in [1, l]$ such that $p_k \in CT_n$,
   (b) for all $k' \in [1, l]$ and $n' \in \mathbb{N}$, $n' \neq n$ implies $p_{k'} \not\in CT_n';$
3. if $S''(\text{Mhd}[n]) = T$, $p_i \in CT_n$, $p_i \not\in S$ and $p_i \not\in D$, then there exists a $T'' \in S_{TM''}$ and $p'_1 \in p_1, \ldots, p'_{n-1} \in p_{n-1}$ such that $(\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i), S'') \overset{+}{\rightarrow} (\|i\|_{\text{ct}(n-1)} \overset{\sim}{\vdash} (p_i) \circ l) \mid (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i))$, $T'' \mid (\text{M}_{\text{tape}} = S'' \mid \text{M}_{\text{tape}}$ and $T''(\text{Mhd}[n]) = T;$
4. if $S''(\text{Mhd}[n]) = T$ and $p_i \equiv CT_n$, then there exists a $T'' \in S_{TM''}$ such that $(\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i), S'') \overset{+}{\rightarrow} (\|i\|_{\text{ct}(n+1)} \overset{\sim}{\vdash} (p_i) \circ l) \mid (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i))$, $T'' \mid (\text{M}_{\text{tape}} = S'' \mid \text{M}_{\text{tape}}$ and $T''(\text{Mhd}[n]) = T;$
5. if $S''(\text{Mhd}[n]) = T$, $p_i \equiv CT_n$ and $S''(\text{Mhd}[n]\{\text{ct}(n), S''(\text{ct}(n))\}) \not\in \{S, D\}$, then:
   (a) if $\pi_2(S''(\text{Mhd}[n]\{\text{ct}(n), S''(\text{ct}(n))\})) = \text{test.s}$, then there exists a $T'' \in S_{TM''}$ such that $(\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i), S'') \overset{+}{\rightarrow} (\|i\|_{\text{ct}(n+1)} \overset{\sim}{\vdash} (p_i) \circ l) \mid (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i))$, $T'' \mid (\text{M}_{\text{tape}} = S'' \mid \text{M}_{\text{tape}}$ and $T''(\text{Mhd}[n]) = T;$
   (b) if $\pi_2(S''(\text{Mhd}[n]\{\text{ct}(n), S''(\text{ct}(n))\})) = \text{write.s}$, then there exists a $T'' \in S_{TM''}$ such that $(\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i), S'') \overset{+}{\rightarrow} (\|i\|_{\text{ct}(n+1)} \overset{\sim}{\vdash} (p_i) \circ l) \mid (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i))$, $T'' \mid (\text{M}_{\text{tape}} = S'' \mid \text{M}_{\text{tape}}$ and $T''(\text{Mhd}[n]) = T;$
   (c) if $\pi_2(S''(\text{Mhd}[n]\{\text{ct}(n), S''(\text{ct}(n))\})) = \text{move.s}$, then there exists a $T'' \in S_{TM''}$ and $p''_2 \in p_2, p'_1 \in p_1$ such that $(\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i), S'') \overset{+}{\rightarrow} (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i) \circ l) \mid (\|i\|_{\text{ct}(n)} \ldots \overset{\sim}{\vdash} (p_i))$, $T'' \mid (\text{M}_{\text{tape}} = S'' \mid \text{M}_{\text{tape}}$ and $T''(\text{Mhd}[n+1]) = T;
(d) if \( \pi_2(S''(M_{thd}[\text{null}(S'', S''(rr))])) = \text{movel} \), then there exist a \( T'' \in S_{TM''} \) and \( p'_2 \in p_2 \), \( p'_1 \in p_1 \) such that \((||_2((p_1) \cdots \circ (p_1)), S'') \vdash_{TM''}^* \langle \langle (CT''_m) \rangle \circ \langle (CT''_n) \rangle, T'' \rangle \) and \( T'' \triangleright (M_{tape} \cup \{rr\}) = I_{\text{movel}}(S'') \) and either \( n > 0 \) and \( T''(M_{hd}[n-1]) = T \) or \( n = 0 \) and \( T''(M_{hd}[n]) = T \).

6. if \( S'''(M_{hd}[n]) = T \), \( p_1 \equiv CT''_n \) and \( S'''(M_{thd}[\text{null}(S'', S''(rr))])) \in \{S, D\} \), then:

(a) if \( S'''(M_{thd}[\text{null}(S'', S''(rr))])) = S \), then there exists a \( T'' \in S_{TM''} \) such that \((||_2((p_1) \circ \cdots \circ (p_1)), S'') \vdash_{TM''}^* (S, T'') \) and \( T'' \triangleright (M_{tape} = S'' \mid M_{tape}) \) and \( T''(M_{hd}[n]) = T \);

(b) if \( S'''(M_{thd}[\text{null}(S'', S''(rr))])) = D \), then there exists a \( T'' \in S_{TM''} \) such that \((||_2((p_1) \circ \cdots \circ (p_1)), S'') \vdash_{TM''}^* (D, T'') \) and \( T'' \triangleright (M_{tape} = S'' \mid M_{tape}) \) and \( T''(M_{hd}[n]) = T \);

7. if \( S'''(M_{hd}[n]) = T \) and \( p_1 \equiv CT''_n \), then there exist a \( T'' \in S_{TM''} \) and \( p'_2 \in p_2 \), \( p'_1 \in p_1 \) such that \((||_2((p_1) \circ \cdots \circ (p_1)), S'') \vdash_{TM''}^* (||_2((CT''_m) \circ (CT''_n) \circ \cdots \circ (CT''_n)) = ||_2(p'_2) \circ (CT''_m), T'' \)) and \( T'' \triangleright (M_{tape} = S'' \mid M_{tape}) \) and \( T''(M_{hd}[n]) = T \).

Property 1 is easily proved by induction on \( m \). Using property 1, property 2 is easily proved by induction on \( n \). Using properties 1 and 2, property 3 is easily proved by case distinction between the different forms \( p_1, \ldots, p_l \) can take. Using properties 1 and 2, the remaining properties are easily proved by case distinction between the different forms \( p_2, \ldots, p_l \) can take.

Let \((p_m, S_m)\) be the \( m \)-th element in the full path of \( p \cdot TM S_0 \). Let \((p'_m, S''_m)\) be the first element in the full path of \( ||_2(\langle CT_0 \rangle) \cdot TM'' S''_m \) and let \((p''_{m+1}, S'''_{m+1})\) be the element in the full path of \( ||_2(\langle CT_0 \rangle) \cdot TM'' S''_m \) that follows the \( m \)-th element of which the first component equals \( ||_2(\text{exsba}_{\alpha} \circ CT''_n) \) for some \( n \in \mathbb{N} \) and \( \alpha \in \mathcal{T}_{\text{move}}^* \). Then, using the above equations and other properties, it is straightforward to prove by induction on \( m \) that:

- \( p_m \) is represented by the part of \( s_{thd}(p) \) to which \( \text{null}(S''_m, S''(rr)) \) points;
- \( S_m \mid (M_{tape} \cup \{rr\}) = S''_m \mid (M_{tape} \cup \{rr\}) \) and for all \( n \in \mathbb{N} \), \( S_m(\text{head}) = n \) iff \( S''_m(M_{hd}[n]) = T \).

(for \( m < |p \cdot TM S_0| \) if \( p \cdot TM S_0 \) is convergent). From this, the theorem follows immediately.

The way to simulate Turing machines on a Maurer machine described in this section involves interleaving of the threads in a thread vector. The thread vector concerned consists of finite-state threads only. Initially, the thread vector consists of one thread. The length of the thread vector usually increases during execution. However, we conclude from Theorem 3 and the definition of the apply operator that it remains finite if the computation concerned is convergent.

In Section 8, the instructions used to simulate Turing machines includes instructions with an infinite input region and instructions with an infinite output region. In Section 9, only instructions with a finite input region and a finite output region are used together with adapted Turing threads. However, another kind of infinity arises: the adaptation turns many Turing threads, which are finite-state threads, into infinite-state threads. In this section, the adaptation of

22
Turing threads is circumvented by storing the Turing threads and then executing the stored Turing threads under control of a multi-thread that makes the head position part of the instructions. By using thread forking in the way described, the execution remains controlled by a finite-state thread if the computation concerned is convergent. However, still another kind of infinity arises: the thread forking function needed is an injective function with an infinite domain, viz. \( \mathbb{N} \).

### 11 Fair Strategic Interleaving

Cyclic interleaving with perfect forking is a simple instance of a fair interleaving strategy. In this section, we make precise what it means for basic interleaving strategies with support of perfect forking to be fair. It happens that the way to simulate Turing machines on a Maurer machine presented in Section 10 works with any fair basic interleaving strategy with support of perfect forking.

In [3], it is demonstrated that it is in essence open-ended what counts as an interleaving strategy. However, here we have to make precise what we consider to be an interleaving strategy. Our choice is conditioned by the simple fact that strategies that are not relevant to the present purpose can be left out. This means that we consider only basic interleaving strategies with support of perfect forking, but without support of other special features. For instance, we do not consider interleaving strategies that support the case where processing of certain actions may be temporarily blocked and/or blocked forever. And we do not consider any kind of non-perfect forking either.

A basic strategic interleaving operator \( \parallel_s(\cdot) \) is an operator on a thread vector such that for all \( \alpha \in T_{\text{finrec}}^* \), \( p', p'' \in T_{\text{finrec}} \), \( a \in A_{\tau} \setminus N_T \) and \( n \in \text{dom}(\phi) \):

\[
\parallel_s(\langle \rangle) = S, \\
\parallel_s(\langle S \rangle \bowtie \alpha) = \parallel_s(\alpha), \\
\parallel_s(\langle D \rangle \bowtie \alpha) = S_0(\parallel_s(\alpha)), \\
\exists! \alpha', \alpha'' \in T_{\text{finrec}}^* \bullet (\alpha' \in \text{perm}(\langle p' \rangle \bowtie \alpha) \land \alpha'' \in \text{perm}(\langle p'' \rangle \bowtie \alpha) \land \\
\parallel_s(\langle y' \leq a \geq y'' \rangle \bowtie \alpha) = \parallel_s(\alpha') \leq a \geq \parallel_s(\alpha'')), \\
\exists! \alpha' \in T_{\text{finrec}}^* \bullet (\alpha' \in \text{perm}(\langle y' \rangle \bowtie \alpha \bowtie \langle \phi(n) \rangle) \land \\
\parallel_s(\langle y' \leq \text{nt}(n) \geq y'' \rangle \bowtie \alpha) = \tau_a \bowtie \parallel_s(\alpha')).
\]

The strategic interleaving operators characterized here basically operate as follows: at each interleaving step, the first thread in the thread vector gets a turn to perform an action and then the remaining thread vector is permuted in a deterministic manner. Hence, for a given basic strategic interleaving operator \( \parallel_s(\cdot) \), the axioms can always be given in the following way:

---

6 We write \( D^* \) for the set of all finite sequences with elements from set \( D \), \( D^+ \) for the set of all non-empty finite sequences with elements from set \( D \), and \( \text{perm}(\alpha) \) for the set of all permutations of sequence \( \alpha \).
where \( a \) stands for an arbitrary member of \( \mathcal{A}_{\text{tau}} \setminus \mathcal{N} \mathcal{T} \), for unary functions \( pp_s^+ \alpha \), \( pp_s^- \alpha \) and \( pp_s^{+\text{nt}(n)} \) on \( \mathcal{T}_{\text{finrec}}^+ \) such that, for all \( \alpha \in \mathcal{T}_{\text{finrec}}^+ \), \( pp_s^+ \alpha (\alpha) \in \text{perm}(\alpha) \), \( pp_s^- \alpha (\alpha) \in \text{perm}(\alpha) \) and \( pp_s^{+\text{nt}(n)}(\alpha) \in \text{perm}(\alpha) \).

In order to determine whether a basic interleaving strategy is fair, we need to know how thread vectors are permuted. If \( \alpha \) is a thread vector in which a thread occurs more than once, we cannot infer from \( \alpha \) and the thread vector resulting from a permutation of \( \alpha \) how \( \alpha \) is permuted. Hence, the functions \( pp_s^+ \alpha \) and \( pp_s^- \alpha \) are not sufficient to determine whether a basic interleaving strategy is fair.

Therefore, we assume that, for all \( \alpha \in \mathcal{A}_{\text{tau}}, b \in \mathcal{A} \setminus \mathcal{N} \mathcal{T} \) and \( \alpha \in \mathcal{T}_{\text{finrec}}^+ \), functions \( pp_s^+ \alpha (\alpha), pp_s^- \alpha (\alpha) : [1,|\alpha|] \rightarrow [1,|\alpha|] \) are given such that:

\[
pp_s^+ \alpha (\alpha_1 \cdots \alpha_n) = \langle p'_1 \cdots p'_n \rangle \Rightarrow \\
\forall i \in [1,n] \cdot p_i \equiv p'_i \equiv \alpha_1^i \cdots \alpha_n^i(\alpha_1 \cdots \alpha_n) ,
\]

\[
pp_s^- \alpha (\alpha_1 \cdots \alpha_n) = \langle p'_1 \cdots p'_n \rangle \Rightarrow \\
\forall i \in [1,n] \cdot p_i \equiv p'_i \equiv \alpha_1^i \cdots \alpha_n^i(\alpha_1 \cdots \alpha_n) .
\]

Auxiliary relations \( \alpha \xrightarrow{+^a} \alpha' \) and \( \alpha \xrightarrow{-^a} \alpha' \) for \( \alpha \in \mathcal{A}_{\text{tau}} \), and \( \alpha \xrightarrow{+^{\text{nt}(n)}} \alpha' \), \( \alpha \xrightarrow{-^{\text{nt}(n)}} \alpha' \), for \( b \in \mathcal{A} \setminus \mathcal{N} \mathcal{T} \), are used below to define fairness of basic interleaving strategies. They are defined as follows:

\[
\alpha \xrightarrow{+^a} \alpha' \iff \\
\exists p, p' \in \mathcal{T}_{\text{finrec}}, \alpha'' \in \mathcal{T}_{\text{finrec}}^+ \cdot \\
(\alpha = \langle p \sqsubseteq a \triangleright p' \rangle \triangleright \alpha'' \land \alpha' = pp_s^+ \alpha (\langle p \rangle \triangleright \alpha'')) \quad \text{if} \ a \notin \mathcal{N} \mathcal{T} ,
\]

\[
\alpha \xrightarrow{+^{\text{nt}(n)}} \alpha' \iff \\
\exists p, p' \in \mathcal{T}_{\text{finrec}}, \alpha'' \in \mathcal{T}_{\text{finrec}}^+ \cdot \\
(\alpha = \langle p \sqsubseteq \text{nt}(n) \triangleright p' \rangle \triangleright \alpha'' \land \alpha' = pp_s^{+\text{nt}(n)}(\langle p \rangle \triangleright \alpha'' \triangleright \langle \phi(n) \rangle)) ,
\]

\[
\alpha \xrightarrow{-^a} \alpha' \iff \\
\exists p, p' \in \mathcal{T}_{\text{finrec}}, \alpha'' \in \mathcal{T}_{\text{finrec}}^+ \cdot \\
(\alpha = \langle p \sqsubseteq b \triangleright p' \rangle \triangleright \alpha'' \land \alpha' = pp_s^- \alpha (\langle p' \rangle \triangleright \alpha'')) .
\]

Let \( \|_{\alpha} (\) \) be a basic strategic interleaving operator. Then \( \|_{\alpha} (\) \) is fair if for all \( \alpha_0, \alpha_1, \ldots \in \mathcal{T}_{\text{finrec}}^+ \) and \( j_0 \in [1,|\alpha_0|], j_1 \in [1,|\alpha_1|], \ldots \):

\[
\bigwedge_{i \in \mathbb{N}} (\exists a \in \mathcal{A}_{\text{tau}} \cdot (\alpha_i \xrightarrow{+^a} \alpha_{i+1} \land pp_s^+ \alpha (a_i) (j_i) = j_{i+1}) \lor \\
\exists a \in \mathcal{A} \setminus \mathcal{N} \mathcal{T} \cdot (\alpha_i \xrightarrow{-^a} \alpha_{i+1} \land pp_s^- \alpha (a_i) (j_i) = j_{i+1}) ) \Rightarrow \bigvee_{i \in \mathbb{N}} j_{i+1} = 1 .
\]
According to the above definitions, cyclic interleaving with perfect forking is a fair basic interleaving strategy. The way to simulate Turing machines on a Maurer machine shown in Section 10 works not only with cyclic interleaving, but also with any other fair basic interleaving strategy.

**Theorem 4.** Theorem 3 goes through if we replace the strategic interleaving operator for cyclic interleaving by any other fair basic interleaving strategy.

*Proof.* The proof follows the same line as the proof of Theorem 3. Properties 4, 5a and 5b from that proof are too strong in the case of an arbitrary fair basic interleaving strategy. We have the following weaker properties instead:

4'. if $S''(\text{M}_{\text{hd}}[n]) = \text{T}$ and $p_1 \equiv \text{CT}_n$, then there exist a $T'' \in \text{S}_{\text{T}}$ and $p'_2 \in p_2, \ldots, p'_2 \in p_2$ such that $(||((p_1) \ldots \rightarrow (p_2))||, S'') \rightarrow_{\text{T}_{\text{TM}}} (||((\text{CT}_{n+1}) \rightarrow (\text{CT}_{n}')) \rightarrow (p_2') \leftarrow \ldots \rightarrow (p_2'))||, T'')$ and $T'' | \text{M}_{\text{tape}} = S'' | \text{M}_{\text{tape}}$ and $T''(\text{M}_{\text{hd}}[n]) = \text{T};$

5'. if $S''(\text{M}_{\text{hd}}[n]) = \text{T}$, $p_1 \equiv \text{CT}_n$, and $S''(\text{M}_{\text{hd}}[\text{ntl}(S'', S''(\text{rr}))]) \notin \{S, D\}$, then:

(a) if $\pi_2(S''(\text{M}_{\text{hd}}[\text{ntl}(S'', S''(\text{rr}))])) = \text{test}: s$, then there exist a $T'' \in \text{S}_{\text{T}}$ and $p'_2 \in p_2, \ldots, p'_2 \in p_2$ such that $(||((p_1) \leftarrow \ldots \rightarrow (p_2))||, S'') \rightarrow_{\text{T}_{\text{TM}}} (||((\text{CT}_{n}')) \leftarrow (p_2') \rightarrow \ldots \rightarrow (p_2'))||, T'')$ and $T'' | (\text{M}_{\text{tape}} \cup \{\text{rr}\}) = I_{\text{test}: s}(S'') | (\text{M}_{\text{tape}} \cup \{\text{rr}\})$ and $T''(\text{M}_{\text{hd}}[n]) = \text{T};$

(b) if $\pi_2(S''(\text{M}_{\text{hd}}[\text{ntl}(S'', S''(\text{rr}))])) = \text{write}: s$, then there exist a $T'' \in \text{S}_{\text{T}}$ and $p'_2 \in p_2, \ldots, p'_2 \in p_2$ such that $(||((p_1) \leftarrow \ldots \rightarrow (p_2))||, S'') \rightarrow_{\text{T}_{\text{TM}}} (||((\text{CT}_{n}')) \leftarrow (p_2') \rightarrow \ldots \rightarrow (p_2'))||, T'')$ and $T'' | (\text{M}_{\text{tape}} \cup \{\text{rr}\}) = I_{\text{write}: s}(S'') | (\text{M}_{\text{tape}} \cup \{\text{rr}\})$ and $T''(\text{M}_{\text{hd}}[n]) = \text{T}.$

These weaker properties are sufficient to complete the proof. □

12 Conclusions

There are many ways to simulate Turing machines on Maurer machines. In this paper, we have presented three ways which give insight into the connections between Turing machines, Maurer machines and real computers:

- In the first way, the Maurer machine on which Turing machines are simulated has the most obvious instructions for the simulation of Turing machines. Moreover, the transition function of the Turing machine in question is rendered in an obvious way into a finite-state thread which is applied to that Maurer machine. Unlike real computers, the Maurer machine used for the simulation has instructions with an infinite input region or an infinite output region.

- In the second way, the Maurer machine on which Turing machines are simulated has only instructions with a finite input region and a finite output region. This is attained by replacing each instruction with an infinite input region or an infinite output region by a countably infinite number of instructions, namely one for each different head position. The necessary adaptation of the thread into which the transition function of a Turing machine is rendered, usually results in an infinite-state thread. Unlike finite-state threads, an infinite-state thread cannot be regarded as the behaviour of a deterministic sequential program under execution on a real computer.

25
In the third way, the Maurer machine on which Turing machines are simulated has again only instructions with a finite input region and a finite output region. However, the thread into which the transition function of a Turing machine is rendered is not adapted, but first stored in the memory of the Maurer machine and then executed under control of a multi-thread that makes the head position part of the instructions. The multi-thread forks off for every head position a control thread of itself on the head reaching the preceding position for the first time. Thus, the multi-thread remains finite in the case of convergent computations.

The third way also illustrates that some main concepts of contemporary programming, namely multi-threads and thread forking, have an interesting theoretical application.

Our interest in Maurer machines originates from our plan to develop, as part of a project investigating micro-threading architectures [10], an approach to design processor architectures that exploit instruction level parallelism. As a first step, we have developed a basic theory of stored threads and their execution based on Maurer machines. The development of that theory is presented in [4]. Like the work presented in this paper, that work also builds upon thread algebra [3]. Our work presented in [5], on a framework for specification and verification of systems that consist of several multi-threaded programs on various hosts in different networks, builds upon thread algebra as well.

References


