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Design, optimization and realization of a 10 GHz static frequency divider.

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ABSTRACT

To demonstrate the performance of a high speed bipolar process a 10 GHz 64:1 static frequency divider has been built. Two types of circuits have been designed and optimized for maximum operating frequency. These are the basic static frequency divider and an alternative static frequency divider. For the basic static frequency divider an expression has been derived that relates the maximum operating frequency to the electrical parameters in the circuit. With this expression not only circuit optimization but also process optimization is possible. Simulations have shown that, after optimization, the maximum operating frequency for the basic frequency divider and for the alternative frequency divider is respectively 11.5 GHz and 12.5 GHz. Layouts have been designed for the frequency dividers. The dividers have been processed and evaluated. The maximum operating frequency that has been measured is 6.6 GHz for the basic static frequency divider and 8.7 GHz for the alternative static frequency divider. The difference between simulated and measured operating frequencies is caused by a process deviation.
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1 INTRODUCTION

To recapture and strengthen the European co-leadership in the field of high speed bipolar technology and circuits, the TIPBASE project has been set up. TIPBASE (Technology Integration Project Bipolar Advanced Silicon for Europe), as one of the large Esprit-2 TIP projects, encompasses the whole spectrum of bipolar activities including bipolar structures and processes, device physics, modeling and simulation, circuit design and CAD tools. The primary goal of the project is to develop a high frequency bipolar process whose performance can be illustrated by a number of technology and pre-production demonstrators. For this purpose Philips, as one of the main industrial contractors, has developed a high frequency bipolar process. To demonstrate the performance of this process, among other demonstrators, a static frequency divider must be built which can deal with a frequency of 10 GHz and a power supply of 5 volt.

In this thesis the design, optimization and realization of such a frequency divider is described. Especially the optimization of the divider, in order to obtain the maximum toggle frequency, is a problem. One can do circuit simulations for optimizing the circuit, but this is time consuming and expensive. A better approach is to derive some sort of expression which relates the maximum toggle frequency to the electrical parameters of the circuit. With this expression the maximum toggle frequency can be predicted and the circuit of the frequency divider can be optimized.

Up till now only one expression is available in the literature that relates the maximum toggle frequency to the electrical parameters of the circuit. But, as we will show in this thesis, a fundamental error has been made in the derivation of this expression resulting in inaccuracy. For this reason a new expression has been derived. First, in chapter 2, the bipolar transistor as one of the basic building blocks of the frequency dividers is examined. The transistor model MEXTRAM used for circuit simulations and properties of high frequency transistors
that will be used are presented.
In chapter 3 a general introduction of the standard static frequency divider is given and some properties of this type of frequency divider are examined.
Chapter 4 deals with the transient analysis of the static frequency divider. We will examine the high frequency operation of the divider and we will derive an expression for the maximum toggle frequency.
In chapter 5 some alternative frequency dividers are presented. The (dis-) advantages of these dividers compared with the static frequency divider are discussed.
Chapter 6 describes the design of the complete frequency divider with the input, buffer and output stages.
Chapter 7 describes the layout design of the circuits.
In chapter 8 the frequency dividers that have been processed are evaluated and the results of the measurements are presented.
Chapter 9 concludes the thesis with conclusions and recommendations.
2 CHARACTERIZATION OF THE BASIC TRANSISTOR

2.1 Introduction

The bipolar npn transistor is the most important building block of the ECL frequency divider. The quality of the transistor determines the performance of the frequency divider. Especially the high frequency operation of the divider, i.e. the maximum toggle frequency, depends on the properties of the transistor. At the PHILIPS RESEARCH LABORATORIES EINDHOVEN a high frequency bipolar process, called BASIC, has been developed. Transistors realized in this technology have qualities that make them suitable for high frequency operation. Therefore the frequency divider will be realized with this technology. Because the transistor is so important understanding its operation at high frequencies is necessary. For describing the behaviour of the transistor a transistor model is needed. This model should not only be accurate but also compact. The accuracy of the model depends on the set of mathematical equations describing the terminal behaviour and on the accuracy of the numerical constants in these equations. These constants are called parameters. Examples of parameters are, among others, the base resistance and the emitter-base depletion capacitance. At Philips an accurate and compact model has been developed. It is called MEXTRAM (Most EXquisite TRAnsistor Model) and will be used for the circuit simulations. The model incorporates many physical effects which are not incorporated in other transistor models such as the Ebers-Moll model and the Gummel-Poon model. It also accounts for the high frequency behaviour of the transistor and is therefore suited for modeling the transistors in the frequency divider. The parameter values are obtained from measurements. For several transistors the electrical parameters of the BASIC transistor have been extracted.
In section 2.2 a overview will be given of the MEXTRAM model. In section 2.3 the electrical parameters which characterize the BASIC transistor are presented. In addition some properties of the BASIC transistor are examined.

2.2 The MEXTRAM model

The transistor model MEXTRAM which is used in the Philips circuit simulation programs is a rather extensive model. We will only give a brief overview of the MEXTRAM model for the npn transistor. We first examine the npn transistor then present the MEXTRAM equivalent circuit and a simplified circuit.

2.2.1 The npn transistor

In figure 2.1 a typical npn transistor is shown with indicated the series resistances and depletion capacitances. Some resistances and depletion capacitances are separated into intrinsic (i) and extrinsic (x) parts. In the intrinsic part, under the emitter, the main current flows.

Shown are the base-emitter depletion capacitance \((C_{ei}, C_{ex})\), the base-collector depletion capacitance \((C_{ci}, C_{cx})\) and the collector-substrate capacitance \((C_s)\). Also shown are the emitter resistance \((R_e)\), the base resistance \((R_{bc}, R_{bv})\) and the collector resistance \((R_{cc}, R_{cv})\). Because the intrinsic base and collector resistance are current dependant they are called \(R_{bv}\) and \(R_{cv}\) (\(v\) of variable). The extrinsic resistances \(R_{bc}\) and \(R_{cc}\) are constant (\(c\) of constant).

The value of \(R_{cv}\) is influenced only at high currents when (quasi-) saturation occurs. In practice this situation will be avoided. The intrinsic base resistance is a strong function of the current.
In particular it decreases markedly at high base currents. The decrease in $R_{bv}$ is caused by current crowding due to the lateral flow of base current underneath the emitter. The lateral flow of base current $I_b$ results in an $I_bR$ voltage drop along the width of the emitter resulting in a varying base-emitter voltage $V_{be}$ with distance. $V_{be}$ will be the highest at the emitter edge closest to the base contact. Since the emitter current depends exponentially on $V_{be}$ a small lateral voltage drop gives rise to a large variation in emitter current along the width of the emitter. In fact the emitter current crowds towards the base contact resulting in a lower $R_{bv}$. Current crowding can decrease $R_{bv}$ by a factor 2 or more at high currents.

2.2.2 The MEXTRAM equivalent transistor circuit

In this section we will restrict our attention to the equivalent circuit diagram of the MEXTRAM model for the npn transistor. In figure 2.2 the equivalent circuit of the MEXTRAM transistor model is shown. For a comprehensive description of the model, the model equations and the underlying physics the reader is referred to [1], [2] and [3]. The topology of the circuit resembles the Gummel-Poon model but with the addition of extra nodes. The extra nodes have been added
fig. 2.2 Equivalent circuit of the MEXTRAM transistor model

to account for the intrinsic and extrinsic part of the transistor. From the Gummel-Poon model the forward and reverse currents ($I_r$ and $I_r$) and the base currents ($I_{b1}$, $I_{b2}$ and $I_{b3}$) are known. Extra is the current $X_{b1}$ which models the side wall component of the base current.

The depletion capacitances are represented by their depletion charges $Q_t$.

The charge in the neutral base, due to the minority carrier concentrations, is modeled by $Q_{bc}$ and $Q_{be}$. In addition to these charges $Q_n$ and $Q_{ep}$ model the charge stored in respectively the neutral emitter and the collector epilayer.

Avalanche multiplication is modeled by the current source $I_{avl}$ and
parasitic substrate current is modeled by $I_{\text{sub}}$.
The current dependence of the intrinsic base resistance is modeled by a diode connected in parallel with $R_{\text{bV}}$. The current dependence of the intrinsic collector resistance $R_{\text{cv}}$ is modeled by the voltage source $E_{C}+dE_{C}$. $R_{\text{bV}}$ and $R_{\text{cv}}$ are the low current values.
Finally the pn junction diodes between base-collector and substrate-collector with the currents $I_{\text{ex}}$ and $I_{\text{sf}}$ are shown.

2.2.3 The simplified MEXTRAM equivalent transistor circuit

For the transistors in the frequency divider the extensive circuit shown in figure 2.2 can be simplified. The simplified circuit is shown in figure 2.3. Simplification is possible because for the transistors in the frequency divider the following statements yield:

a) the transistors are forward biased. Thus the collector-base voltage $V_{\text{cb}}$ is positive. Hence no (quasi-) saturation occurs.
b) the substrate is connected to the lowest voltage in the circuit.
c) $V_{\text{cb}}$ is less than the breakdown voltage.

From a) it follows that the reverse current $I_{r}$ and therefore also the reverse base current $I_{\text{b3}}$ is zero. This also implies that $Q_{\text{bc}}$ and $Q_{\text{ep1}}$ are zero. With the base-collector junction reverse biased $I_{\text{ex}}$ is zero. Without saturation $R_{\text{cv}}$ is not modulated so $E_{C}+dE_{C}$ is zero. And without saturation $I_{\text{sub}}$ is zero.
From b) it follows that the substrate-collector junction is reverse biased. So $I_{\text{sf}}$ is zero.
From c) it follows that $I_{\text{av1}}$ is zero.
fig. 2.3 Simplified equivalent circuit of the MEXTRAM transistor model
2.3 Properties of the BASIC transistor

The transistors in the frequency divider will be realized in the BASIC process. BASIC (Best Alignment with SIdewall Contact) offers a lithography independent self-aligned fabrication of the emitter and base region. Due to this self-alignment the extrinsic area can be reduced resulting in much lower base resistance and smaller capacitances [4], [5]. In figure 2.4 an example is given of an idealized self-aligned BASIC transistor.

Besides the self-alignment, deep trench isolation (indicated as 'oxide' in figure 2.4) has been applied. This isolation has replaced the traditional collector-base junction isolation (see figure 2.1) and results in a lower collector-base capacitance.

fig. 2.4 Schematic illustration of the layout of an idealized, self-aligned BASIC transistor. (a) plan view; (b) cross-sectional view
Typical for the BASIC transistor is that the intrinsic part of the collector-base capacitance is much smaller than the extrinsic part. A double base contact has been used for reducing the base resistance even more.

2.3.1 The electrical parameters of the BASIC transistor

From the BASIC transistor the MEXTRAM parameters have been extracted. Because several parameters are geometry dependant the parameters have been extracted for transistors with different emitter widths \( w \) and emitter lengths \( l \). Measured are the electrical parameters for \( w=0.35, 0.85, 1.35, 1.85 \) and \( 2.35 \) \( \mu \text{m} \) and for \( l=8.85, 18.85 \) and \( 48.85 \) \( \mu \text{m} \). Several of these geometry dependant parameters, the series resistances and the zero biased depletion capacitances are shown in figure 2.5. The markers show the measured parameter values.

In order to obtain parameter values for other than the measured \( w \) and \( l \), parameter functions have been derived which approximate the measured parameter values. These parameter functions are continuous functions of \( w \) and \( l \) and will be used for circuit simulations. In figure 2.5 the parameter functions are represented by the solid lines. The values of \( R_{bv} \) and \( R_{cv} \) are the low current values.

In addition to the measured MEXTRAM parameters the Charge-control model parameter \( T_r \) (forward transit time) is shown in figure 2.6. The parameter \( T_r \) is not measured but calculated using the MEXTRAM model. In appendix B this calculation has been carried out. The parameter \( T_r \) will be used for circuit analysis.

A remark must be made about the parameter extraction. For a reliable parameter extraction, for each \( w \) and \( l \) many transistors should be measured on different wafers. This would result in a set of typical parameter values for that geometry. For the BASIC process only a few transistors have been measured on one wafer, so the typical parameter values could be higher or lower.
fig. 2.5 Various measured MEXTRAM parameters
fig. 2.5 various measured MEXTRAM parameters (continued)
fig. 2.5 Various measured MEXTRAM parameters (continued)
fig. 2.6 The calculated Charge Control parameter $T_r$
2.3.2 BASIC transistor measurements

For characterization of the BASIC transistor and for verification of the MEXTRAM model several AC and DC measurements have been carried out. Three of them we will examine as they provide information that is relevant for the design of the divider. These are the DC current gain $h_{re}$, the base-emitter voltage $V_{be}$ and the cut-off frequency $f_T$. The cut-off frequency is the frequency where the AC small signal current gain is equal to one. It is a figure of merit for the high frequency performance of the transistor.

The measurement results are shown in figures 2.7, 2.8 and 2.9. The quantities have been measured for a transistor with $w=0.85 \, \mu m$ and $l=18.85 \, \mu m$. The markers represent the measured values, the solid lines the results obtained with the MEXTRAM model. It can be seen that, except for the cut-off frequency, the MEXTRAM model is quite accurate. For the cut-off frequency the MEXTRAM model gives somewhat too low values.

In figure 2.8 and 2.9 it can be seen that for high currents the transistor performance decreases because both $h_{re}$ and $f_T$ decrease. This is caused by high-injection effects [1], [3]. The usable current range is below the critical current $I_{crit}$ where the high-injection starts. This is the low-injection regime. For this transistor $I_{crit} = 6 \, mA$ which corresponds with the critical current density $J_{crit} = \frac{I_{crit}}{w \cdot l} = 0.4 \, mA/\mu m^2$. For other transistor geometries $J_{crit}$ has also been calculated resulting in the same value for $J_{crit}$.

For the best high frequency performance the current density $J$ should also be not too low because of the decrease of $f_T$ at low current densities. From figure 2.9 it follows that by reducing the current density from $J_{crit}$ to $J_{crit}/10$ the $f_T$ halves. This is also true for the other transistor geometries. Therefore the usable current density range is $0.04 \, mA/\mu m^2 < J < 0.4 \, mA/\mu m^2$.

In this current range the DC current gain exceeds 100 for every transistor geometry. From figure 2.7 it can be seen that for $J = 0.04 \, mA/\mu m^2$ $V_{be} = 0.79 \, volt$ and for $J = 0.4 \, mA/\mu m^2$ $V_{be} = 0.85 \, volt$, independent of the transistor geometry.
fig. 2.7 The base-emitter voltage versus base and collector current

fig. 2.8 DC current gain versus the collector current
fig. 2.9 The cut-off frequency versus the collector current
3 BASIC OPERATION OF THE 64:1 FREQUENCY DIVIDER

3.1 Introduction

Frequency dividers are important devices for communication systems and measuring instruments. With advances in gigabit-per-second communication systems, the need for very high speed dividers has become more important [6], [7], [8], [9]. Apart from these applications these circuits are also commonly used to demonstrate the capability of a technology for producing high-speed circuits. To demonstrate the performance of the BASIC technology a frequency divider must be built. This frequency divider has to meet the following requirements:

- It must be realized in a bipolar technology.
- The maximum toggle frequency must be 10 GHz.
- The frequency divider must be built of standard static divider circuits using Emitter Coupled Logic (ECL)
- the power supply must be about 5 volt.
- the input signal must be divided by 16 or more.

Figure 3.1 shows the block diagram of a 64:1 frequency divider. The 64:1 frequency divider divides the input signal by 64. It comprises an input and output stage, 6 frequency divider stages (divide by 2 (1)... divide by 2 (6)) and buffer stages. Each frequency divider stage divides its differential input signals (C\̅C) by two, resulting in the differential output signals (Q\̅Q). Differential signals are used because Emitter Coupled Logic uses differential signals. Unlike the internally used differential signals, the input and output signal are single ended. This is because it is easier to generate a single ended high frequency input signal than a differential high frequency input signal. It also saves external connections.

The input stage converts the single ended input signal into a


Fig. 3.1 Block diagram of the 64:1 frequency divider.

differential signal. This stage also provides the impedance matching necessary for the high frequency input signal. For this reason the input impedance must be 50 Ω.
The output stage converts the differential output signal to the single ended output signal $V_{out}$ and also acts as a buffer with an output impedance of 50 Ω.
Buffer stages connect the dividers. They act not only as buffer but also as level shifter needed for the DC coupling between the frequency dividers.
In this chapter we restrict our attention to the frequency divider stage as the most important part of the 64:1 frequency divider. First we will examine the basic operation of the divider. Then the ECL implementation of the divider will be discussed. The ECL logic, the ECL current switch and the ECL flip-flop, being the essential parts of the ECL frequency divider, will be examined. Finally the ECL divider is presented.
3.2 Basic operation of the frequency divider

In the 64:1 frequency divider six frequency divider stages are present. There are two categories of frequency dividers which have been described in the literature. One is the static frequency divider and the other the dynamic or regenerative frequency divider [10], [11]. The static frequency divider is based on the trigger connected master-slave D-type flip-flop. This type of frequency divider must be realized and will be examined.

In figure 3.2.a the logic circuit diagram of the static frequency divider is shown. The flip-flop in the master (F1a,F1b) and in the slave (F2a,F2b) are shown. They are connected to each other by AND gates (P1a,P1b,P2a,P2b) controlled by the clock signals C and \( \bar{C} \).

When the clock is high (C=1) gates P1a and P1b are open and the data from the slave outputs \( Q \) and \( \bar{Q} \) is set on the inputs of the master flip-flop. The master flip-flop latches these signals. Thus the data is copied from the slave into the master. Notice that due to the cross coupled wires data inversion takes place between slave and master. Therefore \( M \) becomes \( \bar{Q} \) and \( \bar{M} \) becomes \( Q \).

When C=0 data from the master is clocked through gates P2a and P2b and latched in the slave flip-flop.

In this way, during each clock period, the slave outputs change logic state (when C=0). This results in the frequency division by two. In figure 3.2.b the timing sequence of the frequency divider is shown.
fig. 3.2 Static frequency divider. (a) Logic diagram; (b) Timing sequence.
3.3 Emitter Coupled Logic

It is required that the frequency divider uses Emitter Coupled Logic (ECL). This is not surprisingly given the fact that it presently is the fastest available form of digital logic. The reason for this is that transistors in ECL do not saturate and the internally used voltage swings are small compared with other logic families [12].

The basis of all ECL circuits is the nonsaturating current switch shown in figure 3.3. As can be seen from the figure another name for this circuit is the emitter coupled pair. Vee is the negative power supply voltage (Gnd is 0 Volt).

The current switch operates as follows. By applying a sufficient voltage difference \( V_{i1} - V_{i2} \) to the switch the current \( I_q \) can be forced to flow through transistor \( T_1 \) thereby reducing \( I_2 \) to zero. To be more precise, the difference in input voltage can be expressed as \( V_{i1} - V_{i2} = V_{be1} - V_{be2} \).
Using the ideal diode equation

\[ V_{be} = V_T \ln \frac{I_c}{I_o} , \]

with \( I_c \) the collector current, \( V_T \) the thermal voltage (\( V_T = 26 \text{ mV} \) for \( T=300 \text{ K} \)) and \( I_o \) the saturation current we have

\[ V_{11}-V_{12} = V_T \ln \frac{I_1}{I_2} , \]

with \( I_1 \) and \( I_2 \) the collector current through respectively \( T_1 \) and \( T_2 \).

So to cause a 100:1 ratio between \( I_1 \) and \( I_2 \) a voltage difference \( V_{11}-V_{12} \) of 120 \text{ mV} \) is already sufficient. In practice we take this value somewhat higher to compensate for the loss of voltage over the base and emitter resistance. We therefore consider the emitter coupled pair as a current switch when driven with sufficient input voltage. In that case \( T_1 \) is considered to be on with \( I_1=I_q \) and \( T_2 \) is off with \( I_2=0 \).

With the load resistances \( R_1 \) and \( R_2 \) (with \( R_1 = R_2 = R_L \)) the current is converted into the differential output voltage

\[ V_{out} = V_{01}-V_{02} \]

\( V_{out} \) can be expressed as:

\[ |V_{out}| = |V_{01}-V_{02}| = I_qR_l \]

The logic '1' ('0') now correspond with a positive (negative) differential output voltage.

Because the output voltage is applied to the input of other ECL gates we require that the output voltage is large enough so

\[ I_qR_L >120 \text{ mV} . \]

(1)
When the input voltage is too large the collector-base voltage of transistors T1 or T2 may become negative. In that case saturation of the transistors is possible. Therefore, to prevent the case of saturation, a sufficient condition is that the collector-base voltage is always positive. This yields \( V_{01} \geq V_{11} \) and \( V_{02} \geq V_{12} \). Because the lowest value for \( V_{01} \) and \( V_{02} \) is \(-I_qR_L\), the condition to prevent the case of saturation is

\[
V_{11}, V_{12} \leq -I_qR_L.
\]  

Thus for application of the current switch we require that (1) and (2) are fulfilled.

### 3.4 The ECL flip-flop

The flip-flop is one of the essential parts of the divider. As discussed in section 3.2 the flip-flop is preceded by a gate, so that data can be clocked in the flip-flop at discrete-time moments. The combination of the gate and the flip-flop is called the clocked flip-flop. Both the master and the slave are in fact clocked flip-flops. The ECL implementation of the clocked flip-flop is subject of this section. In figure 3.4 the ECL implementation of the slave is shown. The implementation of the master is identical. In this figure the input clock signals \( C \) and \( \bar{C} \), the input signals \( M \) and \( \bar{M} \) and the output signals \( Q \) and \( \bar{Q} \) correspond with the signals in figure 3.2.a.

We can identify three current switches \( T_{16}/T_{17}, T_{18}/T_{19} \) and \( T_{20}/T_{21} \). The transistors \( T_{16}, T_{17}, T_{18} \) and \( T_{19} \) use \( R_1 \) and \( R_2 \) as load resistor for the current to voltage conversion. Transistors \( T_{18} \) and \( T_{19} \) form the gate of the clocked flip-flop. Transistors \( T_{16} \) and \( T_{17} \) form the flip-flop. The lower current switch \( T_{20}/T_{21} \) controls the gate and the flip-flop operation.

The operation is as follows. When the clock \( C \) is high the current \( I_q \) is directed to the gate (\( T_{18} \) and \( T_{19} \)) which is then enabled. The flip-flop is then disabled. With the gate enabled the input voltage at \( M \) and \( \bar{M} \) yields an output voltage at \( Q \) and \( \bar{Q} \) (when the voltage at \( M \) is low the voltage at \( Q \) becomes high).
When the clock goes low the gate is disabled and the flip-flop enabled. In that case the operation of the flip-flop is as follows: Assume that the voltage at $Q$ is higher than the voltage at $\bar{Q}$. We then have that $T_{17}$ conducts more current than $T_{16}$. This results in a decrease of the voltage at $\bar{Q}$ and increase in voltage at $Q$. By means of this positive feedback the flip-flop reduces the current through $T_{16}$ to zero resulting in the voltages at $Q$ and $\bar{Q}$ to be high and low respectively. In this way the flip-flop latches the input signal. The data at $Q$ and $\bar{Q}$ is stored as long as the clock is low.

![Diagram of the flip-flop](image)

**fig. 3.4** The clocked flip-flop in ECL

For high speed operation the transistors are not allowed to saturate. For $T_{16}$ and $T_{17}$ however this situation may occur. It can be easily verified that when $T_{16}$ ($T_{17}$) conducts all current the collector-base voltage of $T_{16}$ ($T_{17}$) equals $-I_g R_1$. Therefore level
shifters must be added between output Q and the base of T16 and between output $\bar{Q}$ and the base of T17. Also for high speed operation a buffer is needed between output Q ($Q$) and the base of T16 (T17). As can be seen in figure 3.4 output Q is connected to the base of T17. When the voltage at node Q goes high (T16 in cut-off mode) base current is supplied to T17. This current flows from the voltage source Vcc through R1 in the base. So the output impedance is R1 which can be high resulting in a slow turning on of T17. The buffer guarantees a low output impedance and high driving capability. The well known emitter follower can be used both for level shifting and for buffering.

3.5 The ECL frequency divider

Cascading two clocked flip-flops, described in section 3.4, and connecting the outputs of the second stage to the inputs of the first stage the ECL implementation of the frequency divider described in section 3.2 is obtained. Figure 3.5 shows the ECL frequency divider. The outputs of the master ($M/\bar{M}$) and slave ($Q/\bar{Q}$) and the clock inputs ($C/\bar{C}$) correspond to the signals in figure 3.2. Emitter followers ($T1,T2,T3,T4,T12,T13,T14,T15$) have been applied for buffering and level shifting. Resistors act as current sources. For extra buffering eight emitter followers have been used in stead of four. The extra buffering is desirable because the outputs $M/\bar{M}$ and $Q/\bar{Q}$ have been connected to the base of two transistors.
fig. 3.5
Static frequency divider in Emitter coupled Logic
4 TRANSIENT ANALYSIS OF THE STATIC FREQUENCY DIVIDER

4.1 Introduction

The static frequency divider as described in chapter 3 must be capable of dividing a 10 GHz (or higher) input signal. This is not an extreme high value. In the literature [18], [19], [20], [21], [22], [23], frequencies have been reported up to 21 GHz. At such high frequencies the behaviour of the transistors is primarily determined by the electrical parameters, the resistors and parasitic capacitors, and the current. Because the divider consists for a large part of transistors, the maximum frequency the divider can handle, the toggle frequency, depends on the electrical parameters and the current.

The circuit of the static frequency divider is prescribed by TIPBASE. The only circuit parameters that can be varied are the geometry of the transistors, the gate current $I_g$, the load resistors $R_l$ and the emitter follower resistors. The lateral dimensions of the transistor (emitter width (W) and emitter length (L)) determine the values of the electrical parameters of the transistor. The gate current determines the current that flows through the current switches and the load resistors. The values of the electrical parameters and load resistors are therefore dependent on the gate current. With resistors the the bias currents of the emitter followers are determined.

The load resistors determine the logic voltage swing $V_l$. The logic voltage swing is related to the gate current as $V_l = I_g R_l$.

Thus the question that arises is how to size the transistors and resistors in order to obtain the prescribed toggle frequency. There are two ways to solve this problem. The first is to do circuit simulations. We vary the various circuit parameters and determine the toggle frequency for each set of parameters. This procedure is continued until we have found the maximum toggle frequency corresponding with the optimal choice for the circuit parameters. The disadvantage of this method is that, because of the many parameters involved ($W_1, W_2, \ldots W_{10}, L_1, L_2, \ldots L_{10}$,

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R1, R2, ..., R7), the simulations can cost a lot of time (and money). Also we obtain no understanding which factors influence the toggle frequency.

A better method is to analyze the transient behaviour of the divider and to derive some sort of expression that relates the toggle frequency to the circuit parameters. With such an expression we can analytically find the optimum set of circuit parameters. In this chapter we are especially interested in the analytical method.

In section 4.2 the switching behaviour of the frequency divider is analyzed. We examine what factors limit the toggle frequency and relate the delays in the circuit to the toggle frequency.

In section 4.3 two methods for calculating the delays in the circuit are discussed. One is an analytical method, using the Charge-control model. The other is the sensitivity analysis, using circuit simulations.

In section 4.4 the optimization procedure for maximum toggle frequency is described. Also suggestions to improve transistors, resulting in a higher toggle frequency, are included.

4.2 Relationship between the toggle frequency and the circuit delays

To understand why the frequency divider stops dividing at a certain frequency, we must examine the way data propagates through the divider. Because of the non-ideal current switches, delays are introduced that limit the speed data can be clocked from master into slave or from slave into master. In figure 4.1.a the functional diagram of the divider is shown. In figure 4.1.b the corresponding timing diagram is shown. In figure 4.1.a only the lower current switches, controlling the gates and flip-flops, are explicitly shown. The gate in the master is active during the same interval as the flip-flop in the slave and vice versa. Therefore \( I_{c1} = I_{c2}' \) and \( I_{c2} = I_{c1}' \). In figure 4.1.b these currents are shown.
Fig. 4.1 Frequency divider. (a) functional diagram; (b) timing diagram.
When the clock goes high (at $t=t_0$) the gate in the master becomes active at $t=t_1$. The time delay $t_1-t_0$ is the turn-on time $t_{on}$. With the gate active, data is clocked from the slave output to the master output. At time $t_{on}$ the data is available at the output of the master. The time it takes to clock the data from the slave output to the master output is the propagation delay $t_p = t_{on}-t_1$.

When the clock goes low, the gate in the slave becomes active at $t_2$ and the data from the master output is set on the slave output, also with delay $t_p = t_{on}-t_2$. Because the master is identical to the slave, the propagation delays are the same.

For proper dividing these delays should not be too large. The time between $t_1$ and $t_2$ is precisely half of the clock period $T$. Hence the data must propagate through the gate in less than half of the clock period. Therefore, a necessary condition for dividing is

$$t_p < T/2. \quad (4.1)$$

Also, for an active gate, the turn-on time must be less than half the clock period. This yields the second condition for dividing

$$t_{on} < T/2. \quad (4.2)$$

The flip-flop does not have direct influence on the delays in the divider. The flip-flop only has to latch the signals. Hence, for proper latching, the loop gain of the flip-flop $G_{rr}$ must be equal or greater than unity to maintain the logic state. This is the third condition for dividing

$$G_{rr} > 1. \quad (4.3)$$

$(4.1)$, $(4.2)$ and $(4.3)$ form the set of conditions that must be fulfilled for proper dividing.
In figure 4.2 simulation results of the divider are shown. Input signal (clock), and output signal (divided by two) can be seen. With increasing clock frequency the divider stops at the toggle frequency. Above the toggle frequency one of the conditions for dividing is not fulfilled anymore.

To understand which of the three conditions is the most important, the frequency divider must be examined in more detail. Figure 4.3.a shows the master part of the divider. Figure 4.3.b shows the corresponding simulated voltages and currents.

The delays from input to output, indicated in figure 4.3.b as $t_{on}$, $t_1$, $t_2$ and $t_3$, are defined as the 50% points of the input and output waveforms. The gate is defined as active when $I_{c1} = I_q/2$.

When the clock becomes positive the gate becomes active after the delay $t_{on}$. With the gate active, the data from the slave output ($V_{s1}-V_{s2}$) is set on the master output. This can be described as follows:

First, assume that $V_{s1}-V_{s2}$ is positive as indicated in figure 4.3.b. In that case transistor $T_3$ conducts current and $I_{c3}$ starts flowing. The delay between $I_{c1}$ and $I_{c3}$ is $t_1$. 

Fig. 4.2 Effect of increasing clock frequency on the divider.
Fig. 4.3.a Master part of the frequency divider.
Fig. 4.3.b Simulated voltages and currents in the master.
Then $I_{c3}$ causes the voltage at node 1, $V_1$, to go negative. The delay between $I_{e3}$ and the differential voltage $V_1-V_2$ is $t_2$. Finally the differential output voltage, $V_{m1}-V_{m2}$, becomes negative after the delay $t_3$ caused by the emitter followers. The delays $t_1$, $t_2$ and $t_3$ together form the propagation delay

$$t_p = t_1 + t_2 + t_3$$, with \hspace{1cm} (4.4)

- $t_1$: delay between $I_{c1}$ and $I_{e3}$
- $t_2$: delay between $I_{e3}$ and $V_1-V_2$
- $t_3$: delay between $V_1-V_2$ and $V_{m1}-V_{m2}$.

The propagation delay comprises three delays. One caused by the current switch, one caused by the parasitics at node 1 and one caused by the emitter followers. The turn-on time is caused by one current switch only. Hence we can assume $t_{on} < t_p$. It then follows that condition (4.2) is fulfilled when (4.1) is fulfilled.

Figure 4.4 confirms this assumption. It shows some simulated voltages and currents in the master with increasing clock frequency. All transistors have the same geometry. It can be seen that the amplitude of the current $I_{e1}$ only slightly decreases. Hence condition (4.2) is fulfilled over the whole frequency range. However, the currents $I_{e3}$ and $I_{e4}$ become smaller with increasing frequency. At $t=2.3$ ns $I_{e3}$ and $I_{e4}$ are so small that the division stops. At this point of time the propagation delay exceeds half the clock period and (4.1) is not fulfilled anymore. This validates the assumption that $t_{on} < t_p$. 

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Fig. 4.4 Effect of increasing clock frequency on waveforms in the master.

Condition (4.3) seems also less important than condition (4.1). In figure 4.3.b it can be seen that, when the flip-flop becomes active (Ic2 at 50%) Vm1-Vm2 becomes more negative. This implies that Grr>=1. This can be verified with a simple calculation:
Consider the small-signal equivalent circuit of the current switch. It is known that the small-signal gain $G$ of the current switch with collector current $I_c$ is

$$G = g_m R_l,$$

with $R_l$ the load resistance and with $g_m$ the transconductance

$$g_m = 40I_c.$$

For the load resistance in the frequency divider we have

$$R_l = V_l/I_q = V_l/(2I_c),$$

with $V_l \geq 0.15$ Volt.

Therefore the small-signal gain is

$$G = g_m R_l = 40I_c V_l/(2I_c) = 20 V_l \geq 3.$$ 

Because the flip-flop is a current switch too we have

$$G_{ff} = G > 3.$$ 

Thus the loop gain exceeds unity and condition (4.3) is fulfilled automatically.

Hence when (4.1) is fulfilled (4.2) and (4.3) are also fulfilled. Thus when $t_p < T/2$ the divider functions. This yields for the toggle frequency

$$f_{\text{toggle}} = \frac{1}{2t_p} \quad (4.5)$$

With (4.4) and (4.5) the toggle frequency is related to the delays in the circuit. The toggle frequency only depends of the upper
part of the divider circuit. Transistors T1 and T2 have no influence on the toggle frequency as long as (4.2) is fulfilled. This has been verified with simulations as follows:

It has been shown that the delay of a current switch can be expressed as the sum of time constants like $R_{bc}C_{te}$, $R_{cc}C_{tc}$ [13], [14]. When the value of an electrical parameter increases the delay increases too. In table 4.1 some simulated toggle frequencies are listed for several values of the electrical parameters of the transistors. All transistors have the same geometry.

<table>
<thead>
<tr>
<th>value electrical parameters</th>
<th>$f_{toggle}$ (GHz.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{bc3,4}$ (Ω) $C_{te3,4}$ (fF) $R_{bc1,2}$ (Ω) $C_{te1,2}$ (fF)</td>
<td></td>
</tr>
<tr>
<td>150 28 150 28</td>
<td>10.0</td>
</tr>
<tr>
<td>300 28 150 28</td>
<td>7.8</td>
</tr>
<tr>
<td>150 56 150 28</td>
<td>8.1</td>
</tr>
<tr>
<td>150 28 300 28</td>
<td>9.8</td>
</tr>
<tr>
<td>150 28 150 56</td>
<td>9.9</td>
</tr>
</tbody>
</table>

Without increased parameters the toggle frequency is 10 GHz. This is shown in the first row in the table.

When $R_{bc3}$ and $R_{bc4}$ are increased from 150 Ω to 300 Ω the toggle frequency becomes 7.8 GHz (see row 2 in table 4.1). When $C_{te3}$ and $C_{te4}$ are increased from 28 fF to 56 fF the toggle frequency becomes 8.1 GHz (see row 3 in table 4.1). It is evident that an increase of the electrical parameters of T3 and T4 causes a considerable decrease of the toggle frequency.

However, when $R_{bc1}$ and $R_{bc2}$ are increased (row 4 in table 4.1) or when $C_{te1}$ and $C_{te2}$ are increased (row 5 in table 4.1) the toggle frequency is almost not influenced. We therefore can conclude that T1 and T2 have almost no influence on the toggle frequency, whereas T3 and T4 have a strong influence on the toggle frequency.

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Since \( T_1 \) and \( T_2 \) have almost no influence on the toggle frequency we can simply choose the geometry of transistors \( T_1 \) and \( T_2 \) equal to the geometry of \( T_3 \) and \( T_4 \). The same is valid for \( T_5 \) and \( T_6 \).

4.3 Derivation of the toggle frequency expression

In section 4.2 the toggle frequency has been related to the propagation delay. Several methods are available for computing the propagation delay. One can use the Ebers-Moll transistor model for computations, but this does not lead to generally applicable explicit solutions [15], [16]. A more appropriate method is the use of the Charge-control transistor model [12], [17]. In appendix C it is shown that, with simple hand computations, delay expressions can be obtained that are the sum of weighted time constants. Although the Charge-control analysis can result in somewhat inaccurate expressions it is a useful technique for estimating the order of magnitude of the various delay contributions. Another method that results in accurate and simple delay expressions is the sensitivity analysis [14], [24], [25]. Disadvantage of this method is that all transistors in the divider must be equal.

For a computation of the propagation delay both the Charge-control analysis and the sensitivity analysis will be used. First in section 4.3.1 the three delay components contributing to the propagation delay will be calculated with the Charge-control model. The influence of the load resistors, the biasing of the emitter followers and the transistor geometry on the propagation delay will be discussed. It will be shown that for maximum toggle frequency all transistors can be chosen identical.

In 4.3.2 an accurate toggle frequency expression will be derived, using the sensitivity analysis, and compared with simulation results.
4.3.1 Delay calculations with Charge-control analysis

The propagation delay comprises the three contributions $t_1$, $t_2$ and $t_3$ as described in section 4.2. To simplify the calculations a step input current (or voltage) is applied and the corresponding delay is calculated. The resistor $R_{hv}$ will be neglected. $R_{hv}$ has little influence on the delay because of current crowding (see appendix C).

First $t_1$, the turn-on time of the current switch $(T_3, T_4)$ will be calculated:

In figure 4.5.a the current switch connected to $R_1$ is shown. In figure 4.5.b the Charge-Control equivalent circuit is shown. The time $t_1$ is calculated using the timing sequence as shown in figure 4.5.c. We assume that $V_c$ is zero. For this situation the calculation of $t_1$ has been carried out in appendix C. That calculation has been done for a situation where the common emitter voltage $V_b$ is $-2.85$ Volt. In the divider $V_b = -3*V_{be} \approx -2.55$ Volt. Because of the small difference we assume that the results of appendix C are valid for the current switch. This yields

$$t_1 = R_{bc3}(0.91C_{tc3} + 0.47C_{tc3} + I_qT_f/V_1) + 0.5V_1C_{tc3}/I_q, \quad (4.7)$$

with $V_1$ the differential voltage swing, $V_1 = I_qR_1$, and $T_f$ the base transit time. This parameter relates the collector current to the base charge. The base transit time can be calculated from the MEXTRAM parameters (see appendix B).

The delay $t_2$ is calculated according to the timing sequence shown in figure 4.5.d:

The delay $t_2$ is caused by parasitic depletion capacitances shown in figure 4.5.b. Not only $C_{tc3}$ and $C_{ts3}$ but also $C_{tc5}$ and $C_{ts5}$ influence the delay. The delay $t_2$ can be calculated as follows:

At $t_c$ $V_1=0$, $V_c=0$, $I_1=0$ and $I_{c3}=I_q$.

At $t_4$ $V_1=-I_qR_1/2$, $V_c=V_1-I_qR_{ec3}$, $I_1=I_q/2$ and $I_{c3}=I_q$.  

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Fig. 4.5 Current switch connected to R1. (a) Electrical circuit; (b) Charge-Control equivalent circuit model; (c) Timing sequence for the calculation of \( t_1 \); (d) Timing sequence for the calculation of \( t_2 \).
From this, with the difference in depletion charge \( \Delta Q_t = Q_t(t_d) - Q_t(t_c) \), we have

\[
\begin{align*}
\Delta Q_{tc3} &= -(I_qR_t/2 + I_qR_{cc3})C_{eqc3} \\
\Delta Q_{tc5} &= -(I_qR_t/2)C_{eqc5}
\end{align*}
\]

\[
\begin{align*}
\Delta Q_{ts3} &= -(I_qR_t/2 + I_qR_{cc3})C_{eqs3} \\
\Delta Q_{ts5} &= -(I_qR_t/2)C_{eqs5}
\end{align*}
\]

The large signal depletion capacitances can be calculated with formula (8) of appendix C. This yields

\[
\begin{align*}
C_{eqc3} &= C_{eqc5} = 0.8C_{tc3} \\
C_{eqs3} &= C_{eqs5} = 0.5C_{ts3}.
\end{align*}
\]

For the average current \( I_1 \) we have

\[
I_1 = \frac{I_1(t_d) + I_1(t_c)}{2} = \frac{I_q}{4}.
\]

Using the Charge-control relation

\[
\int_{t_c}^{t_d} I_1 dt = \int_{t_c}^{t_d} I_{c3} dt + \Delta Q_{tc3} + \Delta Q_{ts3} + \Delta Q_{tc5} + \Delta Q_{ts5}
\]

we obtain, after substitution of the depletion charge expressions and the currents,

\[
t_2 = 1.1R_1C_{tc3} + 0.67R_1C_{ts3} + 1.1R_{cc3}C_{tc3} + 0.67R_{cc3}C_{ts3}, \quad (4.8)
\]

with \( R_1 = V/I_q \).

For the calculation of \( t_3 \), the delay in the emitter followers, we assume that the equivalent Charge-Control model shown in figure 4.6 is valid. This is true when the bias currents are constant (ideal current sources), because in that case there is no change in base-emitter charge.

It can easily be verified that \( t_3 \) is approximately given as

\[
t_3 = 0.7R_{bc7}C_{eqc7} + 0.7R_{bc8}C_{eqc8} = 0.65R_{bc7}C_{tc7} + 0.65R_{bc8}C_{tc8}. \quad (4.9)
\]
Fig. 4.6 The cascaded emitter followers. (a) Simplified Charge-Control equivalent circuit; (b) Timing sequence.
With (4.7), (4.8) and (4.9) we have derived an expression for the propagation delay

\[ t_p = t_1 + t_2 + t_3, \]

with \( t_1 \) according to (4.7), \( t_2 \) according to (4.8) and \( t_3 \) according to (4.9).

For several transistor geometries this expression has been compared with simulation results. In table 4.2 the calculated delays and simulated results are listed. All transistors in the divider have been chosen identical \((W=0.85 \mu m, \ L=8.85 \mu m)\). The bias current of the emitter followers is equal to \( I_q \).

<table>
<thead>
<tr>
<th>( I_q ) (mA)</th>
<th>delay (ps)</th>
<th>calculated</th>
<th>simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>( t_1 )</td>
<td>11</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>( t_2 )</td>
<td>29</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>( t_3 )</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>( t_p )</td>
<td>44</td>
<td>61</td>
</tr>
<tr>
<td>2.6</td>
<td>( t_1 )</td>
<td>15</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>( t_2 )</td>
<td>11</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>( t_3 )</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>( t_p )</td>
<td>30</td>
<td>47</td>
</tr>
</tbody>
</table>
From table 4.2 the following can be observed:

- the calculated delays are too small (about 1.5 times).
- the ratio of the calculated delays $t_1$, $t_2$ and $t_3$ is about the same as the ratio between the simulated delays $t_1$, $t_2$ and $t_3$.
- For low (high) currents $t_2$ ($t_1$) dominates the delay.
  This is because $t_2$ is proportional to $R_1 = V_1/I_q$ and $t_1$ is proportional to $I_q$.
- $t_3$ forms about 10% of the total delay.

Although the expression results in too small delay times, it yields the right order of magnitude of the individual delays and relates the delays to the electrical parameters, the current $I_q$ and the voltage swing.

The optimal value for the voltage swing, resulting in the minimum delay, can be found using the formula for the propagation delay $t_p = t_1 + t_2 + t_3$, with $t_1, t_2$ and $t_3$ according to (4.7), (4.8) and (4.9).

A large voltage swing results in a large $t_2$. A small voltage swing results in a large $t_1$. The optimum value depends on the current and the transistor geometry. Simulations have been performed to investigate the influence of the voltage swing on the propagation delay. For a certain transistor geometry and current the load resistors have been varied, resulting in a varying voltage swing and propagation delay. This experiment has been performed for several geometries and currents. For all these experiments the optimal voltage swing turned out to be 0.2 Volt. For $W=0.85$ and $l=18.85$ the simulation results are shown in table 4.3. When $V_1$ is 100 mV the divider stops because this voltage is not sufficient for switching the current switch on or off.

The value of 0.2 Volt agrees well with values reported in the literature [18], [22], [23] (from 0.18 Volt up to 0.28 Volt).
The theoretically optimal transistor geometry for the emitter followers follows from expression (4.9). The geometry should be chosen that minimizes the time constant $R_{bc}C_{tc}$. However, in practice this delay formula is far too simple. An attempt has been made to find a more accurate expression, but this has been unsuccessful. From simulations it has been observed that $t_3$ depends on the bias current and the load, formed by the current switches. But when the emitter follower transistors are chosen identical to the other transistors, and the bias current corresponds with a current density of $3E-4$ A/µm$^2$, $t_3$ is close to the minimum value. Because $t_3$ forms only 10% of the delay, a better analysis of the emitter followers is not necessary.

In section 4.2 we have found that transistors $T_1, T_2, ..., T_6$ can be chosen equal to each other for maximum toggle frequency. We now have found that the emitter follower transistors can be chosen identical to $T_1, T_2, ..., T_6$. Therefore all transistors can be chosen equal to each other. We also have found that the optimal $V_I$ is 0.2 Volt and we have found the optimal resistor values for the emitter followers. Hence for maximum toggle frequency the transistors and resistors should be sized as follows:

- $W_1=W_2=...=W_{10}$.
- $L_1=L_2=...=L_{10}$.
- $V_I=0.2$ Volt.
- choose the value of the bias current of the emitter followers equal to $W*L*3 \times 10^{-4}$. This yields $R_3$, $R_4$, $R_5$ and $R_6$. 

### Table 4.3 Influence of the voltage swing on the propagation delay $t_p$. $W_{10}=0.85$ µm, $L_{10}=18.85$ µm, $I_g=2.6$ mA

<table>
<thead>
<tr>
<th>$V_I$ (V)</th>
<th>simulated $t_p$ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.10</td>
<td>--</td>
</tr>
<tr>
<td>0.15</td>
<td>52</td>
</tr>
<tr>
<td>0.20</td>
<td>46</td>
</tr>
<tr>
<td>0.30</td>
<td>47</td>
</tr>
<tr>
<td>0.40</td>
<td>49</td>
</tr>
<tr>
<td>0.60</td>
<td>52</td>
</tr>
</tbody>
</table>
The remaining unknown circuit parameters are $W$, $L$ and $I_q$.

4.3.2 Derivation of an accurate propagation delay expression

With all transistors in the divider identical, the sensitivity analysis described in [24] and [25] is suitable for calculating the toggle frequency. The sensitivity analysis is based on the fact that the propagation delay of bipolar logic circuits can be expressed as a linear combination of the time constants of the circuit, with each time constant being weighted by a factor that is determined by the circuit topology.

For the frequency divider, assuming that all the time constants of the circuit contribute to the propagation delay, the delay is given by

$$t_p = K_0 T_\text{r} + R_b C_t C_t C_t + K_2 C_t C_t C_t + K_3 C_t C_t C_t + K_4 C_t C_t C_t + K_5 C_t C_t C_t + K_6 C_d$$

$$+ R_b C_t C_t C_t + K_7 C_t C_t C_t + K_8 C_t C_t C_t + K_9 C_t C_t C_t + K_{10} C_t C_t C_t + K_{11} C_t C_t C_t + K_{12} C_d$$

$$+ R_b C_t C_t C_t + K_{13} C_t C_t C_t + K_{14} C_t C_t C_t + K_{15} C_t C_t C_t + K_{16} C_t C_t C_t + K_{17} C_t C_t C_t + K_{18} C_d$$

$$+ R_b C_t C_t C_t + K_{19} C_t C_t C_t + K_{20} C_t C_t C_t + K_{21} C_t C_t C_t + K_{22} C_t C_t C_t + K_{23} C_t C_t C_t + K_{24} C_d$$

$$+ R_b C_t C_t C_t + K_{25} C_t C_t C_t + K_{26} C_t C_t C_t + K_{27} C_t C_t C_t + K_{28} C_t C_t C_t + K_{29} C_t C_t C_t + K_{30} C_d$$

$$+ R_b C_t C_t C_t + K_{31} C_t C_t C_t + K_{32} C_t C_t C_t + K_{33} C_t C_t C_t + K_{34} C_t C_t C_t + K_{35} C_t C_t C_t + K_{36} C_d$$

$$+ R_b C_t C_t C_t + K_{37} C_t C_t C_t + K_{38} C_t C_t C_t + K_{39} C_t C_t C_t + K_{40} C_t C_t C_t + K_{41} C_t C_t C_t + K_{42} C_d$$

$$+ R_b C_t C_t C_t + K_{43} C_t C_t C_t + K_{44} C_t C_t C_t + K_{45} C_t C_t C_t + K_{46} C_t C_t C_t + K_{47} C_t C_t C_t + K_{48} C_d),$$

where $C_{t_t}$, $C_{t_e}$, $C_{t_s}$ are the zero bias depletion capacitances, $R_{b1}$ and $R_{b2}$ are the emitter follower resistances, $R_1$ the load resistance and $C_d$ the diffusion capacitance. In the literature [24], [25] the diffusion capacitance $C_d$ is defined as

$$C_d = \Delta Q_b / (\Delta V_1 / 2).$$

$\Delta Q_b$ is the change in base charge in a asymmetrical current switch with current $I_q$ when switched from off to on. $\Delta V_1 / 2$ is the associated change in input voltage. $V_1$ is the voltage swing $V_1 =$
I_{gR1}. Hence for $C_d$ we obtain, using the relation $Q_b$ (on)=$I_gT_r$ and $Q_b$(off)=0 (see appendix B)

$$C_d = \frac{I_gT_r}{(I_gR_1/2)} = \frac{2T_r}{R_1}.$$ 

The parameter $T_r$, the base transit time, is not a MEXTRAM parameter but it can be calculated from the MEXTRAM parameters (see appendix B).

The propagation delay expression can be simplified considerably. It is seen in the literature [14] that the emitter follower resistance terms are negligibly small and can be eliminated from the propagation delay expression. It is also found that the terms $R_1C_d$ are redundant because $C_d=2T_r/R_1$. Therefore, a simplified propagation delay expression is obtained

$$t_p = K_0T_r + R_{bc}(K_1C_{tc1} + K_2C_{tx} + K_3C_{te1} + K_4C_{tx} + K_5C_{ts} + K_6C_d) + R_{cv}(K_7C_{tc1} + K_8C_{tx} + K_9C_{te1} + K_{10}C_{tx} + K_{11}C_{ts} + K_{12}C_d) + R_{cc}(K_{13}C_{tc1} + K_{14}C_{tx} + K_{15}C_{te1} + K_{16}C_{tx} + K_{17}C_{ts} + K_{18}C_d) + R_{ce}(K_{19}C_{tc1} + K_{20}C_{tx} + K_{21}C_{te1} + K_{22}C_{tx} + K_{23}C_{ts} + K_{24}C_d) + R_e(K_{25}C_{tc1} + K_{26}C_{tx} + K_{27}C_{te1} + K_{28}C_{tx} + K_{29}C_{ts} + K_{30}C_d) + R_t(K_{31}C_{tc1} + K_{32}C_{tx} + K_{33}C_{te1} + K_{34}C_{tx} + K_{35}C_{ts}). \quad (4.10)$$

The remaining 36 weighting factors in (4.10) can be determined by the sensitivity analysis. For example, in order to determine the value of $K_2$, we can apply the second partial derivatives to both sides of the $t_p$ expression (4.10)

$$\frac{\delta^2 t_p}{\delta R_{bc} \delta C_{tx}} = 0 + 0 + K_2 + 0 + \ldots + 0. \quad (4.11)$$

Hence, the method to get the weighting factor $K_2$ can be worked out as follows by means of circuit simulations: increase the value of $R_{bc}$ from $R_{bc1}$ to $R_{bc2}$ at a certain $C_{tx}=C_{tx1}$, run the simulation program and evaluate the difference in $t_p$:

$$\Delta t_p = (R_{bc2}-R_{bc1})(K_1C_{tc1} + K_2C_{tx1} + K_3C_{te1} + K_4C_{tx} + K_5C_{ts} + K_6C_d)$$
The same simulation program can be run at a higher $C_{tx}=C_{tx2}$ to give another similar equation:

$$\Delta t_{p2} = (R_{bc2} - R_{bc1}) (K_1C_{tcl} + K_2C_{tx2} + K_3C_{tx1} + K_4C_{tx} + K_5C_{t} + K_6C_d)$$

Now, by subtracting $\Delta t_{p1}$ from $\Delta t_{p2}$ the following expression is obtained:

$$\Delta t_{p2} - \Delta t_{p1} = K_2(R_{bc2} - R_{bc1})(C_{tx2} - C_{tx1}),$$

which can be rewritten as

$$K_2 = \frac{\Delta t_{p2} - \Delta t_{p1}}{(R_{bc2} - R_{bc1})(C_{tx2} - C_{tx1})} = \frac{\Delta(\Delta t_p)}{\Delta R_{bc}\Delta C_{tx}} = \frac{\delta t_p}{\delta R_{bc}\delta C_{tx}} \quad (4.12)$$

This is just (4.11). Similarly, most other weighting factors can also be determined by variation of the electrical parameters. Only the weighting factors for $C_d$ and $K_0$ are determined in a different way.

The diffusion capacitance, not an electrical parameter, can be varied using the relation $C_d=2T_c/R_1$. With $T_c$ proportional to $T_{ne}$, see appendix B, we can vary $C_d$ by varying $T_{ne}$.

The weighting factor $K_0$ can simply be calculated after all the other weighting factors have been determined. Then $K_0$ follows from

$$K_0 = (t_p - K_1R_{bc}C_{tx} - \ldots - K_3R_1C_{tx})/T_r.$$
Vin1-Vin2 going positive and Vem1-Vem2 going negative is measured. In this way \( t_d \) comprises the four delays that have been discussed in section 4.2

\[
t_d = t_{on} + t_1 + t_2 + t_3.
\]

This delay \( t_d \) is then defined as the propagation delay that is related to the toggle frequency as \( t_d = 1/2f_{toggle} \).

But as we have seen in section 4.2 \( t_{on} \) has no influence on the toggle frequency. Therefore this propagation delay expression yields too high values for the delay.

With several simulations the propagation delay expression, published in [24], has been compared with simulation results. For all simulations the formula resulted in far too high values. Two examples are shown in table 4.4.

<table>
<thead>
<tr>
<th>( W(\mu m) )</th>
<th>( L(\mu m) )</th>
<th>( I_g(\mu m) )</th>
<th>propagation delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.85</td>
<td>8.85</td>
<td>2.6</td>
<td>74 calculated</td>
</tr>
<tr>
<td>0.85</td>
<td>8.85</td>
<td>0.75</td>
<td>92 calculated</td>
</tr>
</tbody>
</table>

Because of the inaccurate expression in [24] a new expression has been derived. This has been done as follows:

Consider the complete frequency divider. In order to determine a weighting factor, for example \( K_2 \), run the simulation program for \( R_{bc1} \) and \( C_{tx1} \) and determine the toggle frequency \( f_{toggle1} \). This can be done with a frequency sweep as shown in figure 4.2. The propagation delay \( t_{p1} \) follows from \( t_{p1} = 1/2f_{toggle1} \). The same simulation program can be run at a higher base resistance \( R_{bc2} \) resulting in \( f_{toggle2} \) and \( t_{p2} \). This yields \( \Delta t_{p1} = t_{p2} - t_{p1} \). Repeat
this for a higher \( Ctcx = Ctx2 \). This yields \( \Delta tp2 \). In this way, with (4.12), the weighting factors can be determined.

With this method all effects, that occur in the frequency divider and influence the toggle frequency, are comprised in the weighting factors of the formula. In table 4.5 the weighting factors obtained with the method described are listed. From table 4.5, it can be concluded that some weighting factors have a very small value (indicated with '0'). The corresponding time constant has therefore no influence on the delay.

In table 4.6 an overview is displayed of the delay contribution of each time constant. It can be seen that the time constants associated with \( Rbc, Rcc \) and \( Rl \) contribute most to the delay. The contribution of the time constants associated with \( Rv \) and \( Rcv \) is very small. The influence of \( Rbw \) is much smaller than \( Rbc \). This is caused by the strong current crowding (see appendix C).

By inspection of table 4.6, the most important terms of the expression can be identified and therefore the propagation delay can be expressed as

\[
\begin{align*}
\tp &= \frac{1}{2f_{\text{toggle}}} \times 0.9T_r + Rbc\left( 2Ctc + 2.2Cte + 0.53Cd \right) \\
&+ Rcc\left( 3.1Ctc + 0.33Cts \right) \\
&+ Rl\left( 1.9 Ctc + 0.83Cts \right) \\
&+ Rbv\left( 0.11Ctc + 0.1Cte + 0.17Cd \right), \quad (4.13)
\end{align*}
\]

with

\[
\begin{align*}
Rl &= V_l/I_q = 0.2/I_q \\
Cd &= 2T_r/Rl = 10T_rI_q \\
T_r &= (1 + \frac{\alpha_1 Cte_{1}}{Qb0}) \left[ \frac{0.56}{I_k} (Qb0 + \alpha_1 Cte_{1}) + Tne \right] \quad (4.14)
\end{align*}
\]

where

\[
\begin{align*}
\alpha_1 &= 0.40 \quad \text{for } V_{be} = 0.79 \text{ volt}, \\
\alpha_1 &= 0.48 \quad \text{for } V_{be} = 0.85 \text{ volt}.
\end{align*}
\]

Formula (4.14), calculated in appendix B, relates \( T_r \) to the MEXTRAM parameters.
### Table 4.5 Weighting factors derived with the sensitivity analysis.

<table>
<thead>
<tr>
<th>$K_i$</th>
<th>value</th>
<th>$K_i$</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_0$</td>
<td>0.9</td>
<td>$K_{19}$</td>
<td>1.1</td>
</tr>
<tr>
<td>$K_1$</td>
<td>2.1</td>
<td>$K_{20}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_2$</td>
<td>2.0</td>
<td>$K_{21}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_3$</td>
<td>2.5</td>
<td>$K_{22}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_4$</td>
<td>1.9</td>
<td>$K_{23}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_5$</td>
<td>'0'</td>
<td>$K_{24}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_6$</td>
<td>0.53</td>
<td>$K_{25}$</td>
<td>4.6</td>
</tr>
<tr>
<td>$K_7$</td>
<td>0.15</td>
<td>$K_{26}$</td>
<td>4.4</td>
</tr>
<tr>
<td>$K_8$</td>
<td>0.11</td>
<td>$K_{27}$</td>
<td>2.6</td>
</tr>
<tr>
<td>$K_9$</td>
<td>0.1</td>
<td>$K_{28}$</td>
<td>2.4</td>
</tr>
<tr>
<td>$K_{10}$</td>
<td>0.1</td>
<td>$K_{29}$</td>
<td>0.6</td>
</tr>
<tr>
<td>$K_{11}$</td>
<td>0.17</td>
<td>$K_{30}$</td>
<td>0.7</td>
</tr>
<tr>
<td>$K_{12}$</td>
<td>3.4</td>
<td>$K_{31}$</td>
<td>2.3</td>
</tr>
<tr>
<td>$K_{13}$</td>
<td>3.1</td>
<td>$K_{32}$</td>
<td>1.9</td>
</tr>
<tr>
<td>$K_{14}$</td>
<td>'0'</td>
<td>$K_{33}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_{15}$</td>
<td>'0'</td>
<td>$K_{34}$</td>
<td>'0'</td>
</tr>
<tr>
<td>$K_{16}$</td>
<td>0.33</td>
<td>$K_{35}$</td>
<td>0.83</td>
</tr>
<tr>
<td>$K_{17}$</td>
<td>'0'</td>
<td>$K_{36}$</td>
<td>0.86</td>
</tr>
<tr>
<td>$K_{18}$</td>
<td>'0'</td>
<td>$K_{37}$</td>
<td>0.87</td>
</tr>
</tbody>
</table>

### Table 4.6 Contribution of the time constants to the propagation delay.

$W=0.85 \, \mu m$, $L=8.85 \, \mu m$, $I_g=1.5 \, mA$

<table>
<thead>
<tr>
<th>$R_i/C_j$</th>
<th>$C_{tc1}$</th>
<th>$C_{tcx}$</th>
<th>$C_{te1}$</th>
<th>$C_{tx}$</th>
<th>$C_{ts}$</th>
<th>$C_d$</th>
<th>$R_i \Sigma C_j$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{bc}$</td>
<td>4.9</td>
<td>4.9</td>
<td>0.5</td>
<td>5.1</td>
<td>0</td>
<td>5.4</td>
<td>20.8</td>
</tr>
<tr>
<td>$R_{bv}$</td>
<td>0.3</td>
<td>0.2</td>
<td>0.02</td>
<td>0.2</td>
<td>0</td>
<td>1.2</td>
<td>1.9</td>
</tr>
<tr>
<td>$R_{cc}$</td>
<td>0</td>
<td>0</td>
<td>0.2</td>
<td>2.3</td>
<td>1.5</td>
<td>0</td>
<td>4.0</td>
</tr>
<tr>
<td>$R_{cv}$</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
</tr>
<tr>
<td>$Re$</td>
<td>0.2</td>
<td>0.2</td>
<td>0.05</td>
<td>0.4</td>
<td>0.4</td>
<td>0.2</td>
<td>1.5</td>
</tr>
<tr>
<td>$R_l$</td>
<td>0</td>
<td>0</td>
<td>0.46</td>
<td>4.4</td>
<td>11.1</td>
<td>0</td>
<td>16.0</td>
</tr>
</tbody>
</table>

$Tr = 4.1 + 48.8 \, \text{ps}$
In (4.13) $C_{tc}$ is the total base-collector capacitance $C_{tc} = C_{tc1} + C_{tcx}$ and $C_{te}$ is the total base-emitter capacitance $C_{te} = C_{te1} + C_{tex}$. These have been combined because the weighting factors associated with these capacitances are nearly the same. Each parameters in (4.13) is a (complex) function of $W$ and $L$. Therefore the propagation delay is not only a function of the MEXTRAM parameters but is also an implicit function of $W$ and $L$.

The accuracy of the propagation delay expression can be verified by simulations. For several emitter lengths and widths and for several current densities $J$ the simulated toggle frequencies have been registered. The results have been compared with the propagation delay expression. In table 4.7 the calculated and simulated delays are displayed. From table 4.7 it follows that the agreement between predicted and simulated propagation delays is good. The accuracy of the propagation delay expression is better then 10% for all $W$ and $L$. The minimum delay of 45 ps (11.1 GHz.) can be found in the neighbourhood of $W=0.85 \, \mu m$, $L=18.85 \, \mu m$ and $J=0.2 \, mA/\mu m^2$ ($I_g=3.2$ mA). It is noted that this is a flat minimum.
<table>
<thead>
<tr>
<th>W (µm)</th>
<th>L (µm)</th>
<th>J (mA/µm²)</th>
<th>calculated t_p</th>
<th>simulated t_p</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35</td>
<td>8.85</td>
<td>0.1</td>
<td>102</td>
<td>97</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>67</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>54</td>
<td>55</td>
</tr>
<tr>
<td>0.35</td>
<td>18.85</td>
<td>0.1</td>
<td>84</td>
<td>84</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>57</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>48</td>
<td>51</td>
</tr>
<tr>
<td>0.35</td>
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<td>0.1</td>
<td>73</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>53</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>47</td>
<td>46</td>
</tr>
<tr>
<td>0.85</td>
<td>8.85</td>
<td>0.1</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>47</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>46</td>
<td>46</td>
</tr>
<tr>
<td>0.85</td>
<td>18.85</td>
<td>0.1</td>
<td>56</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>46</td>
<td>46</td>
</tr>
<tr>
<td>0.85</td>
<td>48.85</td>
<td>0.1</td>
<td>53</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>46</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>48</td>
<td>47</td>
</tr>
<tr>
<td>1.35</td>
<td>8.85</td>
<td>0.1</td>
<td>56</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>50</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>53</td>
<td>55</td>
</tr>
<tr>
<td>1.35</td>
<td>18.85</td>
<td>0.1</td>
<td>55</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>53</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>58</td>
<td>61</td>
</tr>
<tr>
<td>1.35</td>
<td>48.85</td>
<td>0.1</td>
<td>55</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>55</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>63</td>
<td>65</td>
</tr>
</tbody>
</table>
4.4 Optimization of the frequency divider

In the propagation delay expression (4.13) the current $I_q$ appears both in the denominator ($C_d$) and in the numerator ($R_i$). For high currents the term with $C_d$ dominates, for low currents the term with $R_i$ dominates. In figure 4.7 the influence of the current on the propagation delay is shown. The critical current, above which high injection effects occur (increase of $T_r$), is 2.6 mA. In that area the difference between predicted and simulated delay increases.

![Graph showing the influence of the current on the propagation delay.](image)

**Fig. 4.7** Influence of the current on the propagation delay.

It can be seen that the optimum current $I_q,\text{opt}$ is about 2.5 mA. The optimum can be found by differentiating the right side of (4.13) with respect to $I_q$ and setting it equal to zero

$$\frac{\delta T_p}{\delta I_q} = 0 \rightarrow I_q,\text{opt} = \sqrt{\frac{0.2(1.9C_t + 0.83C_t)}{T_f(5.3R_{bc} + 1.7R_{bv})}}. \quad (4.15)$$
Inserting (4.15) in (4.13) yields the propagation delay for optimum current \( t_{p,\text{opt}} \)

\[
t_{p,\text{opt}} = 0.9T_r + R_{bc}(2C_{tc} + 2.2C_{te}) \]
\[
+ R_{cc}(3.1C_{tc} + 0.33C_{ts}) \]
\[
+ R_{bv}(0.11C_{tc} + 0.1C_{te}) \]
\[
+ 2 \sqrt{0.2T_r(1.9C_{tc} + 0.83C_{ts})(5.3R_{bc} + 1.7R_{bv})}. \tag{4.16}
\]

With (4.16) the propagation delay is only a function of the electrical parameters, hence a function of \( W \) and \( L \) only.

With (4.16) the frequency divider can be optimized as follows: Calculate for \( W \) and \( L \) the electrical parameters and then calculate \( t_{p,\text{opt}} \). Repeat this until the minimum \( t_{p,\text{opt}} \) has been found. For this \( t_{p,\text{opt}} \), corresponding with the optimum \( W=W_{\text{opt}} \) and \( L=L_{\text{opt}} \), the corresponding \( I_{q,\text{opt}} \) can be calculated with (4.15). This has been done for the frequency divider and results in

\[
W_{\text{opt}} = 0.55 \ \mu\text{m} \]
\[
L_{\text{opt}} = 28.5 \ \mu\text{m} \quad \rightarrow \quad t_{p,\text{opt}} = 44.6 \ \text{ps} \quad \rightarrow \quad f_{\text{toggle}} = 11.2 \ \text{GHz}. \]
\[
I_{q,\text{opt}} = 5.1 \ \text{mA}
\]

This is the highest toggle frequency that can be obtained after circuit optimization. To obtain an even higher toggle frequency the transistor process should be improved. This means that the electrical parameters that influence the delay, see formula (4.16), must be lowered.

From formula (4.16) but also from table 4.5 it can be seen that the electrical parameters that cause most of the delay are \( R_{bc} \) and \( T_r \). If we only consider the two dominating time constants in (4.16), the terms with \( R_{bc} \), we obtain the simplified propagation delay \( t_{ps} \)

\[
t_{ps} = \frac{R_{bc}(2C_{tc} + 2.2C_{te})}{T_rR_{bc}(1.9C_{tc} + 0.83C_{ts})}. \tag{4.17}
\]
We can relate \( T_r \) to the more frequently used transition frequency \( f_t \)

\[
T_r \approx \frac{1}{2\pi f_{t,\text{max}}},
\]

with \( f_{t,\text{max}} \) the maximum transition frequency. With this (4.17) becomes

\[
\tau_{ps} = R_b c \left( 2C_{t,c} + 2.2C_{t,s} \right)
+ 0.8 \sqrt{\frac{R_b c \left( 1.9C_{t,c} + 0.83C_{t,s} \right)}{f_{t,\text{max}}}}.
\]

(4.18)

Formula (4.18) can be seen as a figure of merit for the optimized frequency divider. It is evident that for process optimization \( R_b c \) must be decreased and \( f_{t,\text{max}} \) must be increased.

This can be illustrated with reported toggle frequencies by NEC and SIEMENS [22], [23]. In table 4.8 their reported maximum toggle frequencies are compared with the maximum toggle frequency that can be obtained with the BASIC process of PHILIPS. Also shown are the maximum transition frequency and the base resistance. These are the estimated values for a transistor with \( W=0.6 \mu m \) and \( L=10 \mu m \). It is noted that the best result of PHILIPS is based on simulations, whereas NEC and SIEMENS have actually measured the frequency.

It is evident that the 15 GHz. of SIEMENS is primarily a result of the lower base resistance. The 21 GHz. of NEC is both the result of lower base resistance and the higher transition frequency.
Table 4.8 Reported maximum toggle frequencies.

<table>
<thead>
<tr>
<th></th>
<th>SIEMENS</th>
<th>NEC</th>
<th>PHILIPS (BASIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_b$ (Ω)</td>
<td>40</td>
<td>42</td>
<td>140</td>
</tr>
<tr>
<td>$f_{t,\text{max}}$ (GHz.)</td>
<td>14</td>
<td>40</td>
<td>18</td>
</tr>
<tr>
<td>$F_{\text{toggle}}$ (GHz.)</td>
<td>15</td>
<td>21</td>
<td>11.2</td>
</tr>
</tbody>
</table>
5 TRANSIENT ANALYSIS OF ALTERNATIVE STATIC FREQUENCY DIVIDERS

5.1 Introduction

The basic static frequency divider, as described in chapter 3, consists of three building blocks, the standard current switch, the load resistor and the emitter follower. All three, but especially the current switch and load resistor, contribute to the propagation delay. It is therefore interesting to investigate if there are alternative current switches or load circuits that introduce less delay.

In the literature alternative current switches [26], [27], [28], [29], and an alternative load circuit [30] have been described. One alternative current switch and the alternative load circuit will be examined in this chapter.

Apart from these different circuit parts, also a different gate/flip-flop timing control is discussed.

In section 5.2 the influence of the alternative load circuit, the so called active load, is discussed.

In section 5.3 an alternative current switch is examined.

In section 5.4 the alternative gate/flip-flop control is described.

5.2 Frequency divider with active load

In [30] the active load, a resistor with a series diode, has been described. In figure 5.1.b the active load is shown. For comparison the normal load resistor is shown in figure 5.1.a. The diode in the active load is formed by the transistor T1 with the base connected to the collector.

In [30] only a small signal analysis of the active load has been carried out. In this section a simple large signal analysis, using the Charge Control model will be carried out. It will be shown that with the active load a smaller propagation delay and hence a higher toggle frequency is obtained.
Fig. 5.1 Load circuits. (a) load resistor; (b) active load.

Fig. 5.2 Test circuits for analysis of the output voltage. (a) Test circuit with load resistor; (b) Test circuit with active load.
Consider the circuits shown in figure 5.2. In this figure the normal and active load are connected to the current source $I_1$. The current source represents the current from a current switch. In the active load a very simple Charge Control model of the transistor is shown. Only the base resistance $R_{be}$ and the base charge $Q_b$ stored in the diffusion capacitance $C_d$ are considered. The other parasitics are neglected to simplify the calculations.

Assume the current $I_1$ is a rectangular pulse which at time $t_0$ abruptly changes from $0.01*I_g$ to $I_g$, with $I_g$ the gate current. We then are interested in the output voltage.

For the load resistor we simply have for the differential output voltage $V_L$:

$$V_L = V_1(t>_{t_0}) - V_1(t<_{t_0}) = -I_gR_1$$

For the active load the situation is more complicated. When $I_1$ becomes $I_g$ at time $t_0$, first the base charge of $T_1$ must be supplied. Therefore at time $t_0$ $I_1 = dQ_b/dt$. The current $I_1$ also flows through $R_{be}$, hence the current causes a voltage drop of $I_1(R_{be}+R_2)$. When base charge is supplied $I_e = Q_b/T_r$ becomes equal to $I_1$, and the voltage drop caused by $I_1$ is $I_1R_2$. The diffusion capacitance together with the base resistance causes an overshoot in the output voltage.

In the following we will calculate the output voltage of the active load.

For the active load we have, with $h_{re}>>1$

$$I_1 = I_e + dQ_b/dt = I_e + T_r dI_e/dt$$

and

$$V_1 = -(V_{T1} + V_{R2})$$

with $V_{T1}$ the voltage between the collector and emitter of $T_1$ and $V_{R2}$ the voltage drop caused by $R_2$. 

65
For $V_{r1}$ and $V_{r2}$ we have

$$V_{r1} = R_{bc} \frac{dQ_b}{dt} + V_{be1} = TrR_{bc}I_c/dt + V_{be1} \quad (5.3)$$

$$V_{r2} = I_1R_2, \quad (5.4)$$

where we have for $V_{be1}$

$$V_{be1} = V_{be1}(0.01*I_q) \quad t < to \quad (5.5)$$

$$V_{be1} = V_{be1}(I_q) = V_{be1}(0.01*I_q) + 120 \text{ mV} \quad t \geq to. \quad (5.6)$$

Using the Laplace transform we obtain for $(5.1)...(5.6)$

$$I_1(s) = \frac{I_q}{s} \quad (5.7)$$

$$I_1(s) = I_c(s) \frac{1+stR}{s} \quad (5.8)$$

$$V_1(s) = -(TrR_{bc}I_c + V_{be1}(s) + I_1(s)R_2) \quad (5.9)$$

$$V_{be1}(s) = \frac{0.12}{s}. \quad (5.10)$$

Substitution of $(5.7)$, $(5.8)$ and $(5.10)$ in $(5.9)$ yields

$$V_1(s) = -\frac{R_{bc}TrI_q}{1+stR} - \frac{0.12}{s} - \frac{I_qR_2}{s}. \quad (5.11)$$

Hence in the time domain, with the proper initial condition for $V_{be1}$, $V_{be1}(t<to) = V_{be1}(0.01*I_q)$, we obtain

$$V_1(t) =$$

$$-I_q(R_2+R_{bc}-\frac{(t-to)}{Tr})U(t-to) - 0.12 U(t-to) - V_{be1}(0.01*I_q), \quad (5.11)$$

with $U(t)$ the step function.

From $(5.11)$ it is evident that there is an overshoot in the output voltage at time $to$. In figure 5.3 the simulated output voltages are shown for the normal and active load. In this simulation all parasitic effects are included. It can be seen that indeed the overshoot predicted by $(5.11)$ occurs. After the time $3Tr$ the overshoot is almost disappeared.
Fig. 5.3 Simulated output voltages for the two load circuits.

The overshoot results in a temporarily larger output voltage swing. Hence also the voltage swing of the emitter followers, that are connected to the load, is larger. Because of the larger voltage swing the charging and discharging of the parasitic capacitances of the current switches, that are connected to the emitter followers, goes faster (the base current is proportional to the voltage swing). This results in a smaller turn-on and turn-off time of the current switches and hence a smaller propagation delay.

For the differential output voltage $V_L(t)$, the difference in output voltage between $V_1(t<t_0)$ and $V_1(t\geq t_0)$ we have with (5.11)

\[
V_L(t_0) = V_1(t_0) - V_1(t_0) = -(0.12 + (R_2+R_{bc})I_b)
\]

\[
V_L(t_0+3T_r) = V_1(t_0+3T_r) - V_1(t_0) \approx -(0.12 + R_2I_2)
\]
Defining the overshoot as the ratio between \( V_l(t_0) \) and \( V_l(t_0+3T_r) \) we obtain

\[
\text{overshoot} = \frac{V_l(t_0)-V_l(t<t_0)}{V_l(t_0+3T_r)-V_l(t<t_0)} = \frac{0.12 + Ig(R_2+R_{bc})}{0.12 + IgR_2} \\
= 1 + \frac{IgR_{bc}}{0.12+IgR_2} .
\] (5.12)

The overshoot is dependant on \( R_{bc} \) (transistor geometry), \( Ig \) and \( R_2 \).

Several simulations have been carried out for the frequency divider with active load. The influence of the transistor geometry, the gate current and the load resistor \( R_2 \) have been examined. The maximum toggle frequency obtained is 12.5 GHz. In table 5.1 the corresponding component values are shown. It is noted that for the divider with active load the power supply voltage must be increased to account for the extra \( V_{be} \) voltage drop.

<table>
<thead>
<tr>
<th>Table 5.1 list of component values for divider with active load. (see figure 4.3) W,L in ( \mu \text{m} ).</th>
<th>( F_{\text{toggle}, \text{max}} = 12.5 \text{ GHz} ).</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_1 \ldots W_6 = 0.45 )</td>
<td>( L_1 \ldots L_6 = 18.85 )</td>
</tr>
<tr>
<td>( W_7 \ldots W_{10} = 0.85 )</td>
<td>( L_7,L_8 = 16 )</td>
</tr>
<tr>
<td>( L_9,L_{10} = 23 )</td>
<td></td>
</tr>
<tr>
<td>( I_g = 3.4 \text{ mA} )</td>
<td>Active load:</td>
</tr>
<tr>
<td>( R_3,R_6 = 1500 \text{ ( \Omega )} )</td>
<td>( W_1 = 0.45 )</td>
</tr>
<tr>
<td>( R_4,R_5 = 800 \text{ ( \Omega )} )</td>
<td>( L_1 = 18.85 )</td>
</tr>
<tr>
<td>( V_{ee} = -6 \text{ Volt} )</td>
<td>( R_2 = 10 \text{ ( \Omega )} )</td>
</tr>
</tbody>
</table>
5.3 Frequency divider with current switch with cut-off prevention

In the normal current switch, see section 3.3, the transistors operate in two modes, the cut-off mode and the forward active mode. To turn the current switch on, first depletion charge (in the cut-off mode) and then neutral base charge (in the forward active mode) must be supplied. See appendix C for a detailed description of the turn-on sequence. When the cut-off situation can be prevented, only neutral base charge has to be supplied. This reduces the average input capacitance, thereby decreasing both the turn-on/off time and the loading imposed on the driving stage.

Prevention of cut-off can be accomplished by adding a diode and a small bias current $I_a$ to the emitter circuit of each transistor [29]. This is shown in figure 5.4. In this way $T_1$ and $T_2$ always conduct a current $I_a$ upon which the gate current $I_g$ is superimposed. The diodes $T_3$ and $T_4$ now act as switches.

![Fig. 5.4 Current switch with cut-off prevention.](image)
This method however has one main disadvantage. For turning on or off the current switch the differential input voltage $V_{\text{sin}}$ must be larger than in the case of the normal current switch. When a larger voltage swing is required the load resistor must be increased too, hereby increasing the propagation delay.

For the normal current switch we already have calculated in section 3.3 that for a 100:1 ratio in collector currents $V_{\text{sin}}$ must be 120 mV. With the parasitic base and emitter resistances this becomes

$$V_{\text{sin}} \text{ (normal)} > 120 \text{ mV} + I_g R_e + I_g (R_{bc} + R_{ev})/h_{re}.$$  \hfill (5.13)

For the current switch with cut-off prevention we can also calculate the differential input voltage to cause a 100:1 ratio in the collector currents of $T_3$ and $T_4$. For $I_{c3}$ and $I_{c4}$ we can write

$$I_{c3} = \beta I_g$$
$$I_{c4} = (1-\beta) I_g, \quad 0 < \beta < 1.$$  

For $I_s$ we can write

$$I_s = \alpha I_g, \quad \alpha > 0.$$  

Therefore we have for $I_{c1}$ and $I_{c2}$

$$I_{c1} = I_g (\alpha + \beta)$$
$$I_{c2} = I_g (\alpha + 1 - \beta).$$

We are interested in the situation that $I_{c3}/I_{c4} = 100$, hence $\beta \approx 0.99$.

For the differential input voltage we can write

$$V_{\text{sin}} = V_{\text{be}1} + V_{\text{be}3} - V_{\text{be}2} - V_{\text{be}4}.$$
With

\[ V_{be} = V_T \ln(I_c/I_0) \]

we obtain

\[ V_{sin} = V_T [\ln((\alpha+\beta)I_q/I_0) + \ln(\beta I_q/I_0) - \ln((1-\beta)I_q/I_0) \\
- \ln((\alpha+1-\beta)I_q/I_0)] \]

\[ = V_T \ln\left(\frac{(\alpha+\beta)\beta}{(1-\beta)(\alpha+1-\beta)}\right) \approx V_T \ln\left(\frac{\alpha+\beta}{\alpha(1-\beta)}\right). \quad (5.14) \]

From (5.14) it follows that for \( \beta = 0.99 \)

\[ V_{sin} \text{ (cut-off, } \alpha=1) > 140 \text{ mV} \]
\[ V_{sin} \text{ (cut-off, } \alpha=0.1) > 180 \text{ mV}. \]

Including the series resistances and assuming \( \alpha=1 \) and all transistor equal we obtain

\[ V_{sin} \text{ (cut-off, } \alpha=1) > 140 \text{ mV} + 3I_q(R_e+(R_{bc}+R_{bv})/hfe). \quad (5.15) \]

Comparison of (5.15) with (5.13) yields that for the current switch with cut-off prevention an extra differential voltage \( \Delta V_{sin} \) is needed

\[ \Delta V_{sin} = 20 \text{ mV} + 2I_q(R_e+(R_{bc}+R_{bv})/hfe). \quad (5.16) \]

Inserting the numerical parameter values of a transistor with \( W = 0.85 \mu m \) and \( L = 18.85 \mu m \) and with \( I_q = 4 \text{ mA} \), we obtain

\[ \Delta V_{sin} = 20 \text{ mV} + 8\times10^{-3}(3+(85+70)/100) = 56 \text{ mV}. \]

For the frequency divider with current switches with cut-off prevention some simulations have been carried out. It has been observed that for proper division the voltage swing must be higher than 250 mV. For the frequency divider with normal current switch
the voltage swing must be higher than 150 mV. This voltage difference can be explained with (5.16). The highest toggle frequency obtained in the simulations is 8.5 GHz. This is obtained for a voltage swing of 350 mV. This is less than the 11.1 GHz for the normal frequency divider. Apparently the large voltage swing introduces more delay than can be gained with the cut-off prevention. Perhaps that a combination of cut-off prevention and active load (large voltage swings) yields higher toggle frequencies. This has not been investigated.

5.4 Frequency divider with alternative gate and flip-flop control

In the basic frequency divider the gates are as long as active as the flip-flop. In figure 5.5.a the timing sequence of the gates in this situation can be seen. P₁ is the gate in the master, P₂ is the gate in the slave. F₁ is the flip-flop in the master, F₂ is the flip-flop in the slave. One could ask if this is an optimum situation. For example, when we allow the gate to be longer active than the slave, is it then possible that a higher toggle frequency can be obtained. With the help of figure 5.5.b we will see if this is possible. In figure 5.5.b the situation is shown that the gate is active during the time αT, where α is the duty cycle. In this case the flip-flops are longer active than the gates. In section 4.2 we have derived the conditions for proper division. The most important one is that when a gate becomes active data must be present. This means that when P₁ becomes active at t₁ data must be present at the input of P₁. Then, at t₂, the data must have propagated through P₁ and be present at the input of P₂. This yields for the propagation delay tₚ

\[ tₚ < t₂-t₁. \]  

(5.17)

For the situation that the gates are as long as active as the flip-flops we have that \( t₂-t₁ = 0.5 \cdot T \). But for the situation that the gates are longer or shorter active than the flip-flops we also
have that \( t_2 - t_1 = 0.5T \). Therefore condition (5.17) is independent of the duty cycle. Hence, no higher toggle frequency can be obtained. However, a decrease of the toggle frequency is possible. When \( \alpha \) is too small or too large the divider stops, because either the gates or the flip-flops are active too short. Simulations have shown that there is no degradation of the toggle frequency for \( 0.3 < \alpha < 0.7 \). We therefore conclude that a duty cycle of 0.5 is the optimum case resulting in the maximum toggle frequency.

\[
P_1 = \overline{F_1}
\]
\[
P_2 = \overline{F_2}
\]

Fig. 5.5 Timing sequence of gate/flip-flop control. (a) Duty cycle = 0.5; (b) duty cycle \( \not= 0.5 \).
6 CIRCUIT DESIGN OF THE COMPLETE 64:1 FREQUENCY DIVIDER

6.1 Introduction

As described in chapter 3 the complete 64:1 frequency divider comprises an input stage, an output stage, buffer stages and six divider stages. The first divider stage must be carefully optimized with respect to the toggle frequency. For the other five divider stages careful optimization is not necessary. The only condition is that stages 2, 3, 4, 5 and 6 must be capable of handling the input frequency divided by 2, 4, 8, 16, 32 and 64 respectively.

In section 6.2, 6.3 and 6.4 the design of respectively the input stage, the output stage and the transistor current source, used in the frequency divider, will be discussed.

In section 6.5 several designs of the first divider stage are presented.

In section 6.6 the design of the other divider stages is described.

In section 6.7 an overview of the complete design of the 64:1 frequency divider is given.

6.2 Design of the input stage

The input stage has to meet several requirements:

1) It must provide a single ended input. This is desirable from a practical point of view, because differential inputs are difficult to use at high frequencies (> 10 GHz.). It also saves an external connection. Therefore an input stage is necessary.

2) The input impedance must be 50 Ω. This is for impedance matching, necessary for the high frequency input signal.

3) The input stage must supply a DC level, necessary for the next divider stage. As can be seen in figure 3.5 the frequency divider...
inputs C and \( \bar{C} \) are connected to the base of the transistors of the lower current switches. To prevent these transistors from saturation, the maximum voltage at the input, \( \hat{V}_c \), must be lower than the minimum collector voltage of these transistors. From figure 3.5 it can easily be verified that the minimum collector voltage of these transistors is \(-3V_{be} - V_I\), with \( V_{be} \) the base-emitter voltage of the transistors and \( V_I \) the voltage swing. With a typical value for \( V_{be} \) of 0.83 Volt and for \( V_I \) of 0.2 Volt we have that \( \hat{V}_c = -2.7 \) Volt. The input signal \( V_{in} \) is a sine wave with amplitude \( A \), and frequency \( f \) superimposed on the DC level \( V_{dc} \). \( V_{in} \) must be smaller than \( \hat{V}_c \). Therefore

\[
V_{in} = V_{dc} + Asin(2\pi ft) < \hat{V}_c .
\]  

(6.1)

From simulations it has been observed that an amplitude of 0.5 Volt is sufficient to obtain the maximum toggle frequency. We therefore have with (6.1), using the numerical values

\[
V_{dc} + 0.5 \sin(2\pi ft) < -2.7 \text{ Volt} \Rightarrow V_{dc} < -3.2 \text{ Volt}.
\]

There is also a lower limit for the DC level. This is caused by the current source in the divider stage. For a correct operation of the current source enough voltage must be available at the nodes 7 and 16 (see figure 3.5). Therefore for \( V_{dc} \) the value of -3.2 Volt is chosen.

In figure 6.1 the circuit diagram of the input stage is shown that fulfills all three requirements. The transistors \( T_1 \) and \( T_2 \) represent the two current switches of the next divider stage. With \( R_1 \) and \( R_2 \) a simple voltage source is realized that provides the DC voltage of -3.2 Volt for the current switches. \( R_1 \) and \( R_2 \) can be calculated with the relation

\[
V_{dc} = -3.2 = -V_{ee}R_1/(R_1+R_2)= -5 R_1/(R_1+R_2)
\]  

(6.2)
Because the resistive voltage source must supply base current to the current switch \( R_1 \) and \( R_2 \), must not be too high. To reduce the power dissipation \( R_1 \) and \( R_2 \), must also not be too low. As a compromise we take for \( R_1 \) 500 \( \Omega \) and for \( R_2 \) 310 \( \Omega \). With these values (6.2) is fulfilled.

The single-ended input is realized by connecting one side of the current switch, the base of \( T_2 \), to the voltage source. In this way the input signal has only to be applied to the base of \( T_1 \).

The 50 \( \Omega \) input impedance is derived as follows. With the capacitor \( C_1 \), the base of \( T_2 \) is grounded for high-frequency signals. Thus for the high-frequency input signal the input impedance, between Ground and the base of \( T_1 \), must be 50 \( \Omega \). This input impedance is formed by the resistor \( R_0 \) in parallel with the two current switches. When we assume that the differential input impedance of one current switch is approximately \( 2R_{bc} \), hence for two current switches in parallel \( R_{bc} \), the input impedance \( Z_{in} \) is

\[
Z_{in} = \frac{R_0 R_{bc}}{R_0 + R_{bc}} \quad (6.3)
\]

For a commonly used transistor with \( L = 18.85 \mu m \) \( R_{bc} \approx 100 \Omega \). In that case for \( R_0 \) a value of 100 \( \Omega \) is chosen. We then have, with (6.3), that \( Z_{in} = 50 \Omega \).

For a proper high-frequency grounding of the base of \( T_2 \) the impedance of \( C_1 \) must be small enough. A value of 1 pF satisfies. With 1 pF we obtain for the impedance of the capacitor

\[
\left| \frac{1}{2\pi fC_1} \right| = 16 \Omega \quad \text{for} \quad f = 10 \text{ GHz}, \quad C_1 = 1 \text{ pF}.
\]

This value is sufficient low for the 10 GHz input signal. For lower frequencies the impedance increases, but as the frequency decreases the need for proper grounding decreases too.

Simulations have been carried out with the input stage connected to a frequency divider. According to the simulations there was no degradation in the maximum toggle frequency. We can therefore conclude that the input stage functions properly.
Fig. 6.1 Circuit diagram of the input stage connected to a current switch.

6.3 Design of the output stage

The output stage has to meet three requirements:

1) The output stage must convert the differential output signal of the last divider into a single ended output signal. This is desirable as it saves one external connection.

2) The output impedance must be 50 Ω. This is for the impedance matching, necessary for the high frequency output signal.
3) The output voltage swing must be compatible with the ECL voltage swing. This means an output voltage swing, $V_i$, of 450 mV.

The current switch, shown in figure 6.2, meets the requirements. The differential input voltage is transformed into a single ended output signal by resistor $R_i$.

As the output impedance of the current switch is approximately equal to $R_i$ we can simply choose for $R_i$ a value of 50 $\Omega$.

The voltage swing of 450 mV is caused by the current through $R_2$, $I_{R_2}$. We therefore have

$$V_i = 450 \text{ mV} = R_i I_{R_2} = 50 I_{R_2} \Rightarrow I_{R_2} = 9 \text{ mA}.$$  

The current through $R_2$ is determined by the DC voltage at the input of the current switch. As can be seen in figure 6.5 of section 6.6 this voltage is $-1.75$ Volt. Hence the voltage at node 1 is $-1.75 - V_{be} = -2.58$ Volt. This yields for $R_2$

$$R_2 = (V_i - V_{ee})/9 \text{ mA} = (-2.58 - -5)/9 \text{ mA} = 270 \text{ $\Omega$}.$$  

![Fig. 6.2 The output stage.](image-url)
Because of the low output frequency, no optimization with respect to the delay in the current switch is necessary. The only points attention has been paid to are the transistor area and the critical current density. For the transistors T1 and T2 a length of 18.85 μm and a width of 1.35 μm satisfies. With this geometry we have for the current density

\[ J = 9 \text{ mA}/(18.85 \times 1.35) = 0.35 \text{ mA/\mu m}^2 < J_{\text{crit}} = 0.4 \text{ mA/\mu m}^2. \]

### 6.4 Design of the transistor current source

In each divider stage two current sources are needed. In this section a simple current source is described.

In figure 6.3 the current source is shown. It comprises a voltage source with output voltage \( V_{\text{bias}} \) and a voltage to current converter. The voltage source consists of \( R_1, R_2, R_3 \) and \( T_1, T_2 \) and \( T_3 \). With an external voltage, \( V_{\text{ext}} \), the bias voltage can be controlled. The voltage to current converter consists of \( T_c \) and \( R_c \) and supplies the gate current \( I_g \).

![Fig. 6.3 Simple transistor current source.](image-url)
With $V_{bias}$ the current through $R_c$, $I_{Rc}$, is controlled. We assume that for all transistors $h_{fe} \gg 1$ (this is true for the BASIC transistor). Therefore

$$I_g \approx I_{Rc} = \frac{V_c}{R_c} = \frac{(V_{bias} - V_{bec} - V_{ee})}{R_c}, \quad (6.4)$$

where $V_{bec}$ is the base emitter voltage of $T_c$. For $V_c$ we choose a value of 0.2 Volt. Hence

$$V_c = V_{bias} - V_{bec} - V_{ee} = 0.2 \text{ V} \Rightarrow V_{bias} = 0.2 + V_{bec} + V_{ee} \quad (6.5)$$

But for the bias voltage we also have

$$V_{bias} = V_{ee} + V_{be1} + V_{be2} + I_1R_2 - V_{be3}. \quad (6.6)$$

Equating (6.5) and (6.6) yields

$$0.2 + V_{bec} = V_{be1} + V_{be2} - V_{be3} + I_1R_2. \quad (6.7)$$

When we choose $I_1$ and $I_3$ equal to $I_g$ then $V_{be1} = V_{be2} = V_{be3} = V_{bec}$. We then have for (6.6) and (6.7)

$$V_{bias} = V_{ee} + V_{be} + I_gR_2 \quad (6.8)$$

$$I_gR_2 = 0.2 \text{ V}. \quad (6.9)$$

From (6.9) the value for $R_2$ follows. The value of $R_3$ follows from

$$I_3 = (V_{bias} - V_{ee})/R_3 \Rightarrow R_3 = (V_{be} + 0.2)/I_g, \quad (6.10)$$

where (6.8), (6.9) and the relation $I_3=I_g$ have been used. The value of $R_1$ follows from

$$I_1 = (V_{ext} - V_{ee} - 2V_{be})/(R_1 + R_2). \quad (6.11)$$
With \( I_1 = I_q \) and with (6.9) the value for \( R_1 \) is obtained

\[
I_q = I_1 = \frac{(V_{ext} - V_{ee} - 2V_{be})}{(R_1 + 0.2/I_q)} \quad \Rightarrow \quad R_1 = \frac{(V_{ext} - V_{ee} - 2V_{be} - 0.2)}{I_q}
\]  

(6.12)

For \( I_q \) a value of 5 mA is chosen, because simulations have shown (see section 6.5) that this value is close to the optimal gate current in the frequency divider. For this current \( V_{be} \) is approximately 0.85 Volt. We can now calculate the resistor values. The calculation has been carried out for \( V_{ext} = 0 \) Volt (connected to ground). This yields for \( R_1, R_2 \) and \( R_3 \), using (6.9), (6.10) and (6.11)

\[
\begin{align*}
R_1 &= 620 \ \Omega \\
R_2 &= 40 \ \Omega \\
R_3 &= 210 \ \Omega
\end{align*}
\]

\[
V_{bias} = 1.05 \text{ Volt} \quad \Rightarrow \quad I_q = 5 \text{ mA} \quad \text{V}_{ext} = 0 \text{ Volt}
\]

For the transistors no optimization has been carried out. For all transistors the emitter length is 10 \( \mu \text{m} \) and the emitter width 1.7 \( \mu \text{m} \). This yields a current density of \( (5 \text{ mA})/(17 \ \mu\text{m}^2) = 0.3 \text{ mA/\mu m}^2 \). This is below the critical current density.

With \( V_{ext} \) not equal to 0 Volt we can vary the current \( I_1 \) and hence the bias voltage and gate current. This may be useful when, due to process variations, the in silicon realized resistors and transistors have different values or geometries. In that case \( I_q \) differs from the calculated value, but with \( V_{ext} \) correction of \( I_q \) is possible.

Simulations have shown that the transistor current source works properly. It showed a gate current of 5 mA as has been calculated. The performance of the frequency divider with the transistor current source was almost as good as with an ideal current source. A slight degradation of the maximum toggle frequency has been observed due to the parasitic capacitances of the current source transistor.
6.5 Designs of the first divider stage

The first divider stages have been carefully optimized with respect to the maximum toggle frequency. Ideally the optimization process described in chapter 4 could have been used for this purpose. However, due to a deadline, first the circuits and the layouts had to be designed. Only after the designs were ready there was time for the derivation of the optimization procedure. Therefore the divider circuits have been optimized by means of extensive simulations. Based on the simulation results the component values and the transistor geometries have been obtained.

It must be noted that parasitic capacitances due to wiring of the layout (see chapter 7) are included in the simulations. These parasitic capacitances have been extracted from the layout designs. It also must be noted that the simulations have been carried out with the input stage, described in section 6.2, connected to the input of the divider. Hence a single ended input signal has been applied.

Several circuit designs have been made for the first divider. These are:

1) The standard frequency divider with a transistor current source
2) The standard frequency divider with a resistor current source
3) The frequency divider with an active load

Design 1 has the advantage over design 2 that the current can be adjusted externally. Design 2 however is simpler and introduces less parasitic capacitances.

Design 3 has been chosen, because from simulations it has been found that with the active load a higher toggle frequency can be obtained than with the resistive load (see chapter 5).
The designs 1 and 2 have been realized in a number of different versions. These versions differ from each other with regard to resistor values and/or transistor geometries. The reason for this is that, because the transistor process BASIC is in an experimental stage, process parameters are constantly varying. This means that the electrical parameter list is subject to changes. This is especially true for the collector-substrate capacitance \( C_{ts} \). It was expected that \( C_{ts} \) could be reduced by a factor 2 or more. Therefore the circuit has been optimized both for the normal \( C_{ts} \) and for the reduced \( C_{ts} \). It was also expected that a 10% reduction in \( R_{bc} \) and a 30% reduction in \( R_{cc} \) could be obtained. For this situation also circuit optimization has been done. For each situation the optimization results in different transistor geometries and hence an other version.

### 6.5.1 Divider stages with transistor current source

The divider stage with transistor current sources is shown in figure 6.4. The frequency divider consists of three parts. The input stage, the divider stage and an output stage. The input stage consists of \( R_{19}, R_{20}, R_{21} \) and \( C_1 \) and was described in section 6.2. Extra is the external connection \( DC_{in} \). With \( DC_{in} \) the DC level can be adjusted if, due to process tolerances, this level is not correct.
Fig. 6.1
Circuit diagram of first divider stage with transistors

Current source.
The output stage is formed by the emitter followers T23, T24, T25 and T26. These emitter followers are necessary for level shifting. It can be seen that the DC voltage at the outputs Q and Q of the divider is \(-2V_{be}-V_{l}/2 = -1.8\) Volt. The DC voltage at the input of the next divider must be lower than \(-3.2\) Volt to prevent the case of saturation (see section 6.2). Therefore with two emitter followers each output voltage is shifted with \(2V_{be} = 1.7\) Volt and results in a DC voltage at S and \(S\) of \(-3.5\) Volt. Apart from level shifting the emitter followers suppress the loading effect of the next divider stage. The sizing of these emitter followers has been done as follows:
Transistors T23 and T24 have been designed with a small geometry and a small current (hence small capacitances) in order to minimize the loading of the divider. T25 and T26 have a larger area and larger bias current in order to obtain a high driving capability for the next stage.
The component values for the input and output stage are listed in table 6.1. By means of simulations it has been verified that the output stage works properly. It provides an excellent level shifting and buffering. However, the extra loading caused by the emitter followers, resulted in a slight decrease in the toggle frequency of about \(0.2\) to \(0.4\) GHz.
The current sources are formed by transistors T11 and T22 with resistors \(R_s\) and \(R_{12}\). The bias voltage BIAS is obtained by the voltage supply described in section 6.4.

Two versions have been simulated for this circuit:

1) Version 'delerA'. This version has been optimized for the normal electrical parameter list as shown in appendix D.
2) Version 'delerB'. This version has been optimized for a reduction in \(C_{ds}\) of 50 %.

After extensive simulations the best component values, resulting in the maximum toggle frequency, have been found. They are listed together with the simulation results in table 6.2 for delerA and in table 6.3 for delerB.
### Table 6.1 Component values for the input and output stage
All resistors in Ω, all W, L in μm.

<table>
<thead>
<tr>
<th>R15</th>
<th>W23=W24= 0.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>R16</td>
<td>W25=W26= 0.85</td>
</tr>
<tr>
<td>R17</td>
<td>L23=L24= 3.85</td>
</tr>
<tr>
<td>R18</td>
<td>L25=L26= 8.85</td>
</tr>
<tr>
<td>R19</td>
<td>C1=1 pF</td>
</tr>
<tr>
<td>R20</td>
<td>310</td>
</tr>
<tr>
<td>R21</td>
<td>100</td>
</tr>
</tbody>
</table>

### Table 6.2 Component values and simulation results for delaerA. All resistors in Ω, all W, L in μm.

| R1=R2=R8=R9  = 50 | W1=W3=W12=W14= 1.05 |
| R3=R7=R10=R14 = 1000 | W2=W4=W13=W15= 1.35 |
| R4=R6=R11=R13 = 500 | W5=W6=W16=W17= 0.6 |
| R5=R12  = 40 | W7=W8=W18=W19= 0.6 |
|            | W9=W10=W20=W21=1.2 |
|            | W11=W22= 1.85 |
| L1=L3=L12=L14 =16.85 |
| L2=L4=L13=L15 =16.85 |
| L5=L6=L16=L17 =23.85 |
| L7=L8=L18=L19 =23.85 |
| L9=L10=L20=L21 =11.85 |
| L11=L22 = 8.85 |

V1=250 mV , Vee = -5 Volt
Ig=5 mA
Simulated f_{toggle} = 10.3 GHz.

### Table 6.3 Component values and simulation results for delaerB. All resistors in Ω, all W, L in μm.

| R1=R2=R8=R9  = 60 | W1=W3=W12=W14= 1.05 |
| R3=R7=R10=R14 = 1000 | W2=W4=W13=W15= 1.35 |
| R4=R6=R11=R13 = 400 | W5=W6=W16=W17= 0.45 |
| R5=R12  = 50 | W7=W8=W18=W19= 0.45 |
|            | W9=W10=W20=W21=0.85 |
|            | W11=W22= 1.85 |
| L1=L3=L12=L14 =16.85 |
| L2=L4=L13=L15 =16.85 |
| L5=L6=L16=L17 =18.85 |
| L7=L8=L18=L19 =18.85 |
| L9=L10=L20=L21 =11.85 |
| L11=L22 = 8.85 |

V1=240 mV , Vee = -5 Volt
Ig=4 mA
Simulated f_{toggle} = 11.2 GHz.

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It can be seen that the toggle frequency for delerB is higher than for delerA. This is caused by the lower collector-substrate capacitance.

It is interesting to compare these results with the best result obtained with the analytical method described in chapter 4. With the analytical method we found that \( f_{\text{toggle}} = 11.2 \text{ GHz.} \) for \( W=0.55 \mu\text{m}, L=28.5 \mu\text{m} \) and \( I_g=5.1 \text{ mA}. \) In delerA the width and length of the most important transistors that contribute to the propagation delay \( (T_7,T_8,T_{18},T_{19}) \) are about the same. Also the gate current agrees well with the analytically found optimal current. This indicates that with the extensive simulations we have obtained a situation that is close to the optimum. The toggle frequency of delerA is however somewhat lower. The difference may be caused by the extra loading of the output stage and the wiring capacitances. With DelerB the toggle frequency is higher, but this is caused by the reduction in \( C_t. \)

6.5.2 Divider stages with resistor current source

The circuit diagram of the divider stage with resistors as current sources is shown in figure 6.2. Except for the current source the circuit is identical to the circuit shown in figure 6.1.

The gate current through \( R_s \) and \( R_{12} \) follows from

\[
I_g = \frac{(V_7-V_{ee})}{R_s} = \frac{(V_{dc}-V_{be}-V_{ee})}{R_s}, \quad (6.13)
\]

where \( V_7 \) is the voltage at node 7 and \( V_{dc} \) the DC voltage of the input stage. The value of \( V_{dc} \) has been designed at \(-3.2 \text{ Volt,} \) \( V_{ee}=-5 \text{ Volt} \) and \( V_{be} \) is approximately \( 0.85 \text{ Volt} \) hence, with these numerical values inserted in (6.13)

\[
I_g = 0.95/R_s. \quad (6.14)
\]

With (6.14) resistor \( R_s \) and \( R_{12} \) can be calculated.
Fig 6.2 Circuit diagram of the first divider stage with resistors as current source.
Two versions have been simulated for this circuit:

1) Version 'delerC'. This version has been optimized for a reduction in $C_t$ of 50%.
2) Version 'delerD'. This version has been optimized for a reduction in $C_t$ of 50%, a reduction in $R_{cc}$ of 30%, and a reduction in $R_{bc}$ of 10%.

After numerous simulations the best component values, resulting in the maximum toggle frequency, have been found. They are listed together with the simulation results in table 6.4 for delerC and in table 6.5 for delerD. The component values of the input and the output stage are the same as for delerA and delerB. They are shown in table 6.1.

The results of delerC are the same as for delerB. This is not surprisingly as the only difference is the current source. From this it follows that the resistor as current source performs as well as the transistor as current source.

The toggle frequency obtained with delerD is the highest, because of the reduction in $C_t$, $R_{bc}$ and $R_{cc}$.

| Table 6.4 component values and simulation results for delerC. All resistors in $\Omega$, all $W,L$ in $\mu m$. |
|---|---|---|
| $R_1=R_2=R_8=R_9=60$ | $W_1=W_3=W_12=W_{14}=1.05$ | $L_1=L_3=L_{12}=L_{14}=16.85$ |
| $R_3=R_7=R_{10}=R_{14}=1000$ | $W_2=W_4=W_{13}=W_{15}=1.35$ | $L_2=L_4=L_{13}=L_{15}=23.85$ |
| $R_4=R_6=R_{11}=R_{13}=400$ | $W_5=W_6=W_{16}=W_{17}=0.45$ | $L_5=L_6=L_{16}=L_{17}=18.85$ |
| $R_5=R_{12}=240$ | $W_7=W_8=W_{18}=W_{19}=0.45$ | $L_7=L_8=L_{18}=L_{19}=18.85$ |
| | $W_9=W_{10}=W_{20}=W_{21}=0.85$ | $L_9=L_{10}=L_{20}=L_{21}=11.85$ |

$V_1=240$ mV, $V_{ee}=-5$ Volt
$I_g=4$ mA
Simulated $f_{\text{toggle}}=11.2$ GHz.
Table 6.5 component values and simulation results for delerD. All resistors in Ω, all W,L in μm.

| R1=R2=R8=R9 | W1=W3=W12=W14 | L1=L3=L12=L14 |
| R3=R7=R10=R14 | W2=W4=W13=W15 | L2=L4=L13=L15 |
| R4=R6=R11=R13 | W5=W6=W16=W17 | L5=L6=L16=L17 |
| R5=R12 | W7=W8=W18=W19 | L7=L8=L18=L19 |

V1=200 mV, Vee = -5 Volt
Iq=4 mA
Simulated f_{toggle} = 11.5 GHz.

6.5.3 Divider stage with active load

In figure 6.3 the frequency divider with active load is shown. For this divider the component values and best simulation results have already been listed in table 5.1. Simulations have been done for only one version that is called delerE. For completeness the component values and simulation results are shown in table 6.6. The active load causes a voltage swing of 400 mV.

Table 6.6 component values and simulation results for delerE. All resistors in Ω, all W,L in μm.

| R1=R2=R8=R9 | W1=W3=W12=W14 | L1=L3=L12=L14 |
| R3=R7=R10=R14 | W2=W4=W13=W15 | L2=L4=L13=L15 |
| R4=R6=R11=R13 | W5=W6=W16=W17 | L5=L6=L16=L17 |
| R5=R12 | W7=W8=W18=W19 | L7=L8=L18=L19 |

V1=400 mV, Vee=-6 Volt
Iq=3.4 mA
Simulated f_{toggle} = 12.5 GHz.
Fig. 6.3 Circuit diagram of the first diode stage with active load.
6.6 Design of the other divider stages

The second, third, fourth, fifth and sixth frequency divider stage do not have an input stage. They only consist of the divider with the output stage (buffer/levelshifter). In figure 6.4 the circuit diagram of the second, third, fourth and fifth divider stage is shown. In figure 6.5 the circuit diagram of the sixth divider stage is shown. The sixth stage has the current switch, described in section 6.3, as output stage. The other divider stages have the buffer/levelshifter as output stage.

It can be seen in figure 6.4 that the output stage consists of one emitter follower with a series diode. With this construction the voltage shift is the same, but the driving capability is less. Only in the first divider stage a high driving capability is needed. In this way we have saved two resistors. The value of R15 and R16 has been designed at 1500 Ω.

For simplicity all the transistors in divider stage 2...6 have been chosen equal to each other. Also all the emitter follower resistors have been chosen equal.

The divider stages have been optimized with regard to power dissipation and area. Therefore the current and the transistor area is kept small. Simulations have been done to find the minimum current and hence the load resistance.

For the second stage the value for the load resistor and the gate current have been designed at respectively 250 Ω and 1.3 mA. For the third, fourth, fifth and sixth stage these values are respectively 500 Ω and 0.4 mA.

Because the second stage must be capable of handling higher input frequency signals than the third, fourth, fifth and sixth stage the current is somewhat higher and the load resistor somewhat smaller. The toggle frequency of the second stage is 7.5 GHz. The toggle frequency of the 3th, 4th, 5th and 6th stage is 4 GHz. In table 6.7 the component values of the divider stages are listed.
Fig. 6.4 Circuit diagram of divider stage 2.5.
6.7 The complete 64:1 frequency divider

The complete frequency divider consists of the divider stages 1...6. For the complete divider simulations have been carried out. It has been found that connecting the 2nd...6th divider stage to the first divider stage has no influence on the the toggle frequency. This means that the output stage of the first divider is not influenced by the loading of the 2nd...6th stage completely. Hence the simulated toggle frequencies for delerA...delerE are also valid for the complete 64:1 divider.

In figure 6.6 the output voltages for the 64:1 frequency divider with delerD as first stage is shown. The output waveforms of each divider stage are shown. The input frequency is 11.5 GHz. The output frequency is 11.5 GHz./64 = 180 MHz.

<table>
<thead>
<tr>
<th></th>
<th>divider stage 2</th>
<th>divider stage 3,4,5,6</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1=R2=R8=R9</td>
<td>250</td>
<td>500</td>
</tr>
<tr>
<td>R3=R7=R10=R14</td>
<td>4000</td>
<td>4000</td>
</tr>
<tr>
<td>R4=R6=R11=R13</td>
<td>1500</td>
<td>1500</td>
</tr>
<tr>
<td>R5=R12</td>
<td>730</td>
<td>2400</td>
</tr>
<tr>
<td>W</td>
<td>1.05</td>
<td>1.05</td>
</tr>
<tr>
<td>L</td>
<td>8.85</td>
<td>8.85</td>
</tr>
</tbody>
</table>

Table 6.7 Component values of divider stage 2...6. All transistors have the same geometry. All resistors in Ω, W,L in µm. Vee = -5 V.
Fig. 6.6 Output waveforms in the 64:1 frequency divider.
7 LAYOUT DESIGNS OF THE COMPLETE 64:1 FREQUENCY DIVIDER

7.1 Introduction

In this chapter the design of the frequency divider layouts is described briefly.
First in section 7.2 some properties of the bipolar process are given. Then in section 7.3 points to pay attention to in the layout design are discussed. And finally in section 7.4 the layout designs are presented.

7.2 Properties of the bipolar process

The bipolar process BASIC is optimized for low voltage (about 5 Volt) and high speed operation. The process offers:

- npn transistors
- polysilicon resistors
- two aluminium metallization layers called IN (INterconnect) and INS (INterconnect Second)

The lateral dimensions of the transistors, the emitter width W and emitter length L, can be varied in order to obtain the desired geometry. In figure 7.1 a transistor layout is shown. Indicated is the double base contact, the emitter contact and the remote collector plug.
In figure 7.2 a typical polysilicon resistor is shown. Indicated are the length Lr and the width Wr of the polysilicon. The ratio between Lr and Wr determines the poly resistance Rp:

\[ R_p = R_s L_r / W_r. \]

Here \( R_s \) is the sheet resistance of the polysilicon. For the BASIC process \( R_s = 276 \ \Omega/\square \).
Not only the poly resistance but also the contact resistance $R_{co}$, caused by the connection of the polysilicon to the interconnect, contributes to the resistance. Therefore the total resistance of the polysilicon resistor is

$$R = R_sL_r/W_r + 2R_{co}.$$  

With the polysilicon resistor most of the resistors in the frequency divider can be made. Only for very small resistor values ($< 20 \Omega$) IN is used.

Fig. 7.1 Layout design of a transistor with double base contact.

Fig. 7.2 Layout design of polysilicon resistor.
On-chip capacitors can be realized using the two metallization layers IN and INS. By stacking the two layers, separated by an oxide layer, so called MIM (Metal Insulation Metal) capacitors are obtained.

7.3 Directions for layout design

The layout design, especially of the first divider stage, must be carried out carefully in order to operate at very high frequency. Parasitic capacitances and resistances, introduced by the interconnect and the transistors and resistors, should be kept as small as possible. Therefore attention has been paid to the following:

- All interconnection lengths are as small as possible to minimize the capacitance between interconnect and substrate.
- Overlap of IN with INS is avoided where possible to minimize the cross-over capacitances.
- Where possible two transistors are combined and share one common collector. For example in figure 6.1 this is done for transistor pairs (T5 and T7), (T6 and T8), (T16 and T18) and (T17 and T19). This yields a reduction in collector-substrate capacitance.

In figure 7.3 the layout design is shown of the first divider stage shown in figure 6.2. Resistors, transistors and the two metallization layers can be identified. It can be seen that there are four transistor pairs which share one common collector. The input and output signals correspond with the signals in figure 6.2.
Fig. 7.3 Layout design of the first divider stage with resistor current source (see figure 6.2).

7.4 The layout designs of the frequency divider

The layouts of all the frequency dividers described in chapter 6 have been designed. In addition four extra layouts have been designed.

DelerA has been realized in two versions. One version with so called super transistors (DelerA1) and one version with normal transistors (DelerA2).

These super transistors have smaller dimensions than the normal transistors and therefore have smaller parasitic capacitances and resistances. However, in contrast to the normal transistor, it was most uncertain if the super transistors would function. But when
the super transistors function a higher toggle frequency than with normal transistors can be obtained.

Both DelerB and DelerC have been realized in two versions. One version with a load resistance of 60 Ω (DelerB1, DelerC1) and one version with a load resistance of 50 Ω (DelerB2, DelerC2). This has been done because process tolerances can result in resistor values that differ from the designed values. Especially for the load resistors a deviation of the designed value can have much influence on the toggle frequency. It is hoped that, for at least one of the processed circuits, the value of the load resistors is close to the designed value of 60 Ω.

Finally a layout has been designed comprising only the first divider stage and the input and output stage. This layout is called Tweedeler. The reason for this design is the following: If there is a layout or process error, somewhere in stage two, three, four, five or six, Tweedeler still operates. In this way we can at least verify the operation of the first divide-by-two stage, even when the other stages do not function.

All together nine different layouts have been designed resulting in three different topologies. In figure 7.4 these three different topologies are shown. The size of the layouts is 2.5 mm x 0.5 mm.

In figure 7.5.a the die, comprising the TIPBASE demonstrators, is shown. The die not only comprises dividers but also other circuits. In figure 7.5.b the positions of the different circuits is indicated. The dividers are marked with ‘*’.
Fig. 7.4  Layout designs of the dividers. (a) Design for DelerA1, DelerA2, DelerB, DelerB1; (b) Design for DelerC, DelerC1, DelerD, DelerE; (c) Design for Tweedeler.
Fig. 7.5.a Layout design of the die comprising TIPBASE demonstrators.
Fig. 7.5.b  Positions of the circuits. The dividers are marked with ‘*’.
All frequency dividers described in chapter 6 and chapter 7 have been processed. In figure 8.1 the divider chip of DelerD is shown. Visible are the six divider stages and the bond pads. The corresponding layout is shown in figure 7.4.b.
In figure 8.2 the first divider stage is shown. The corresponding layout is shown in figure 7.3.
In figure 8.3 the photomicrograph of the normal and the super transistor is shown. The double base contact and the emitter and collector contacts are clearly visible. The size of the super transistor is smaller than the normal transistor. The distance between the base and emitter and the distance between the collector and the base is smaller. This results in lower base resistance, lower collector resistance and lower collector-substrate capacitance.

Fig. 8.1 Photomicrograph of divider chip DelerD (2.5 mm x 0.5 mm).
For all 64:1 frequency divider chips the toggle frequency has been measured. In figure 8.4 the measurement set-up is shown. A sine wave generator (1.2 GHz...20 GHz, maximum amplitude 1.4 Volt) is used for generation of the input signal. The capacitor of 1 nF is for the AC coupling between the DC biased sine wave signal and the DC biased input stage of the frequency divider. With a high frequency scope both the input and the output signal are measured.
Fig. 8.3 Photomicrograph of BASIC transistor. (a) normal transistor; (b) super transistor.

Fig. 8.4 Measurement set-up for measurement of the toggle frequency.
Measurements have shown that every divider operated properly. Every divider divided the input signal by 64. However, the measured toggle frequencies were lower than the simulated toggle frequencies. In table 8.1 the simulated and measured toggle frequencies are listed. It can be seen that for each divider the ratio between simulated and measured toggle frequency is about $1.5 \div 2$.

<table>
<thead>
<tr>
<th>divider</th>
<th>simulated</th>
<th>measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>DelerA1</td>
<td>10.3</td>
<td>5.9</td>
</tr>
<tr>
<td>DelerA2</td>
<td>10.3</td>
<td>6.5</td>
</tr>
<tr>
<td>DelerB</td>
<td>11.2</td>
<td>6.4</td>
</tr>
<tr>
<td>DelerB1</td>
<td>11.2</td>
<td>6.6</td>
</tr>
<tr>
<td>DelerC</td>
<td>11.2</td>
<td>6.3</td>
</tr>
<tr>
<td>DelerC1</td>
<td>11.2</td>
<td>6.2</td>
</tr>
<tr>
<td>DelerD</td>
<td>11.5</td>
<td>6.5</td>
</tr>
<tr>
<td>DelerE</td>
<td>12.5</td>
<td>8.7</td>
</tr>
</tbody>
</table>

It turned out that the discrepancy was caused by a process deviation. The value of emitter, base and collector resistor in the transistors and the values of the polysilicon resistors were a factor $1.5 \div 2$ too high. It can easily be verified that when these resistor values are inserted in the toggle frequency expression (4.16) the predicted toggle frequency is $1.5 \div 2$ times lower. This agrees well with the results shown in table 8.1. It is expected that when there is no process deviation the measured toggle frequencies will be close to the simulated toggle frequencies.

In the table it can be seen that divider DelerA2 operates at a higher frequency than DelerA1. Probably this is the result of the
super transistors in DelerA2.
As expected the highest toggle frequency is obtained with DelerE (active load). In figure 8.5 the input signal and output signal of DelerE are shown. The input frequency is 8.7 GHz and the output frequency $8.7 \text{ GHz} / 64 = 135 \text{ MHz}$.

![Graph showing input and output signals at 8.7 GHz](image)

**Fig. 8.5** Measured input (top) and output (bottom) signals at 8.7 GHz input frequency for DelerE.
Two types of 64:1 frequency dividers have been designed, optimized for maximum toggle frequency and processed. These are the basic static frequency divider (with resistive loads) and an alternative static frequency divider (with active loads: series diode and resistor).

A transient analysis has been carried out for the basic static frequency divider. The results of this analysis are:

- Only a few transistors in the static frequency divider influence the toggle frequency.
- All transistors can be chosen equal to each other for maximum toggle frequency.
- For maximum toggle frequency the optimal internal voltage swing is 0.2 Volt.

Using the Sensitivity Analysis, an analytical maximum toggle frequency expression has been derived for the basic static frequency divider. This expression relates the maximum toggle frequency to the circuit electrical parameters. It has been verified by simulations that the accuracy of this expression is better than 10%.

With the maximum toggle frequency expression the circuit can be optimized. The optimum transistor geometry (emitter width and emitter length) and the optimum circuit current can be found with this expression.

Also process optimization is possible with the expression. Especially the base resistance and the transition frequency have a significant influence on the toggle frequency. For a higher toggle frequency the base resistance must be decreased and the transition frequency must be increased.

Simulations have shown that, after circuit optimization, the maximum toggle frequency for the basic static frequency divider is 11.5 GHz.
The maximum simulated toggle frequency for the alternative static frequency divider is 12.5 GHz. Hence application of the active load results in an increase in toggle frequency.

All processed 64:1 frequency dividers function. The maximum toggle frequency that has been measured is 6.6 GHz for the basic static frequency divider and 8.7 GHz for the alternative static frequency divider. The difference between simulated and measured operating frequency is caused by a process deviation.

The following items are object of further research:

- The influence of the emitter followers and the flip-flop on the toggle frequency.
- Sensitivity Analysis for the alternative static frequency divider.
- Analysis of a static frequency divider with both active loads and current switches with cut-off prevention.
APPENDIX A REFERENCES


APPENDIX B  
CALCULATION OF THE FORWARD TRANSIT TIME FROM THE MEXTRAM MODEL

For transient circuit analysis and computations it is convenient to know the relation between the neutral base charge of the minority carriers in the transistor and the collector current. In the Charge-control model (like the Gummel-Poon model), suited for analytical computations, the forward or base transit time $T_r$ relates to the neutral base charge of the minority carriers $Q_b$ and the collector current $I_c$ as

$$Q_b = T_r I_c \quad (1)$$

In the MEXTRAM model there is no explicit expression available for $T_r$. Therefore we have to calculate $T_r$ by means of the MEXTRAM model equations [1], [2]. We assume that the transistors operate in the low-injection region as is the case in the frequency divider.

In the MEXTRAM model the total neutral base charge is made up of two contributions

$$Q_b = Q_{be} + Q_{ne} \quad (2)$$

Here $Q_{be}$ represents the minority charge in the neutral base and $Q_{ne}$ represents the minority charge in the transition region near the emitter-base junction. $Q_{ne}$ is called the neutral emitter charge. Thus $T_r$ can be calculated using (1) and (2) as

$$T_r = \frac{Q_{be} + Q_{ne}}{I_c} \quad (3)$$

For the low-injection regime $T_r$ is constant and only geometry dependant. This implies that both $Q_{be}$ and $Q_{ne}$ are proportional to $I_c$. In MEXTRAM expressions are available for $Q_{be}$ and $Q_{ne}$. In the following we will first derive an expression for $Q_{be}$ and then for $Q_{ne}$.
In MEXTRAM the neutral base charge is expressed as

\[ Q_{\text{be}} = A_1 N_0 (Q_{\text{bo}} + Q_{\text{tel}} + Q_{\text{tc}}) \]  

where \( Q_{\text{bo}} \) is the zero bias base charge, \( Q_{\text{tel}} \) and \( Q_{\text{tc}} \) are the intrinsic depletion charges of the base-emitter and the base-collector junction respectively. \( N_0 \) is the normalized concentration of the minority carriers:

\[ N_0 = \frac{N(0)}{\hat{N}_A} \]  

with \( N(0) \) the carrier concentration at the edge of the neutral base near the base-emitter junction and \( \hat{N}_A \) the maximum base impurity concentration. The constant \( A_1 \) is expressed as

\[ A_1 = \frac{(\eta-1)e^{2\eta} + e^{\eta}}{(e^{\eta}-1)^2} \]  

with \( \eta \) a measure of the strength of the built-in field in the base due to the graded doping profile.

In figure 1 a typical doping profile of a npn transistor is shown which illustrates the charge distribution for a transistor with base width \( W_b \).

**fig. 1** Typical doping profile in a npn transistor. Hatched areas denote depletion regions.
In MEXTRAM $\eta$, $Q_{bo}$ and $\hat{N}_A$ are parameters. Therefore in (4) only $Q_{te}$, $Q_{te}$ and $N_0$ have to be calculated. For the depletion charges the following relations apply:

\[ Q_{te1} = \alpha_1 C_{te1} \], with $\alpha_1 = \frac{V_{de}(1-(1- \frac{V_{be}}{V_{de}})^{1-p_e})}{1-p_c}$ \hspace{1cm} (7)

\[ Q_{te2} = \alpha_2 C_{te2} \], with $\alpha_2 = \frac{V_{dc}(1-(1- \frac{V_{bc}}{V_{dc}})^{1-p_c})}{1-p_c}$ \hspace{1cm} (8)

Here the parameters $C_{te1}$ and $C_{te2}$ are the intrinsic zero bias depletion capacitances. The parameters $p_e$ and $p_c$ are the grading coefficients of the base-emitter and the base-collector junctions respectively. The parameters $V_{de}$ and $V_{dc}$ are the built-in junction voltages of respectively the base-emitter and the base-collector junctions. $V_{be}$ is the base-emitter voltage and $V_{bc}$ the base-collector voltage.

Thus, with $V_{be}$ and $V_{bc}$ known and the parameters from MEXTRAM, $Q_{te1}$ and $Q_{te2}$ can be calculated.

The normalized carrier concentration $N_0$ follows from the MEXTRAM equation which relates $N_0$ to the collector current $I_c$ as:

\[ I_c(1+ \frac{Q_{te1}+Q_{te2}}{Q_{bo}}) = \frac{N_0}{A_2^2} I_k \], with $A_2 = \frac{2}{\eta} \frac{e^{\frac{\eta-1}{\eta}}}{e^\eta}$ \hspace{1cm} (9)

The knee current $I_k$ is a MEXTRAM parameter.

Expression (9) can be solved for $N_0$. Substitution of $N_0$, (6), (7) and (8) in (4) then yields:

\[ Q_{be} = \frac{4(\eta-1)}{\eta^2 I_k} \frac{Q_{bo}(1+ \frac{Q_{te1}+Q_{te2}}{Q_{bo}})^2}{I_c} \] \hspace{1cm} (10)
In MEXTRAM the neutral emitter charge $Q_{ne}$ is given as:

$$Q_{ne} = \frac{V_{be}}{M_{v}V_{t}} e^{\frac{V_{be}}{M_{v}V_{t}}}.$$  \hspace{1cm} (11)

Here $M_{v}$ is a MEXTRAM parameter and equal to one for the BASIC transistor. $T_{ne}$ is the neutral emitter transit time and $I_{s}$ is the saturation current. Both $T_{ne}$ and $I_{s}$ are MEXTRAM parameters. $V_{t}$ is the well known thermal voltage ($V_{t} = 26 \text{ mV}$ for $T = 300 \text{ K}$).

To eliminate $V_{be}$ in (11) we use the MEXTRAM relation:

$$\frac{V_{be}}{M_{v}V_{t}} e^{\frac{V_{be}}{M_{v}V_{t}}} = \frac{I_{k}}{A_{2}I_{s}} N_{o}. \hspace{1cm} (12)$$

Substitution of (12) in (11) and using (9) yields:

$$Q_{ne} = \frac{T_{ne}I_{k}N_{o}}{A_{2}^{2}I_{s}} = T_{ne}(1+ \frac{Q_{te1}+Q_{tc1}}{Q_{bo}})I_{c}. \hspace{1cm} (13)$$

We now have expressions for $Q_{be}$ and $Q_{ne}$ which are proportional to $I_{c}$. Substitution of (10) and (13) in (3) yields the general formula for the forward transit time:

$$T_{f} = (1+ \frac{Q_{te1}+Q_{tc1}}{Q_{bo}}) \left[ \frac{4(n-1)}{\eta^{2}I_{k}} \left( \frac{Q_{bo}+Q_{te1}+Q_{tc1}}{Q_{bo}} \right) + T_{ne} \right]. \hspace{1cm} (14)$$

$Q_{bo}$, $I_{k}$ and $T_{ne}$ are MEXTRAM parameters. $Q_{te1}$ and $Q_{tc1}$ follow from (7) and (8).

For the BASIC transistor, used in the frequency divider, expression (14) can be simplified. To do so we first examine the typical values of $V_{be}$, $Q_{te1}$ and $Q_{tc1}$ of the BASIC transistor. These values are shown in table 1 for a low and high current density ($J=0.04 \text{ mA}/\mu \text{m}^{2}$ and $J=0.4 \text{ mA}/\mu \text{m}^{2}$) and several geometries. We assume that $V_{bc} = -1 \text{ volt}$.
Table 1 shows that $Q_{tcl}$ is much smaller than $Q_{tel}$. The reason for this is that the intrinsic part of the collector-base capacitance in the self-aligned BASIC transistor is small compared with the intrinsic part of the emitter-base capacitance. Table 1 also shows that $V_{be}$ is only dependant of the current density and is about 0.8 volt. Therefore we can simplify (14) by neglecting $Q_{tcl}$ and using the numeric parameter values of table 1. This results in a simplified formula for the forward transit time $T_r$:

$$T_r = \left(1 + \frac{\alpha_1 C_{tel}}{Q_{bo}}\right) \left[ \frac{0.56}{I_k} (Q_{bo} + \alpha_1 C_{tel}) + T_{ne} \right] , \quad (15)$$

with $\alpha_1 = 0.40$ for $V_{be} = 0.79$ volt ,
$\alpha_1 = 0.48$ for $V_{be} = 0.85$ volt .

The parameters $C_{tel}$, $Q_{bo}$, $I_k$ and $T_{ne}$ are geometry dependant. Table 2 shows $T_r$ for several geometries and current densities. It can be

<table>
<thead>
<tr>
<th>emitter-width (\mu m)</th>
<th>emitter-length (\mu m)</th>
<th>current density (mA/\mu m^2)</th>
<th>$V_{be}$ (V)</th>
<th>$Q_{tel}$ (fC)</th>
<th>$Q_{tcl}$ (fC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35</td>
<td>10</td>
<td>0.04</td>
<td>0.79</td>
<td>8.4</td>
<td>-0.6</td>
</tr>
<tr>
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<td>10</td>
<td>0.4</td>
<td>0.85</td>
<td>9.4</td>
<td>-0.6</td>
</tr>
<tr>
<td>0.85</td>
<td>10</td>
<td>0.04</td>
<td>0.79</td>
<td>13</td>
<td>-1.3</td>
</tr>
<tr>
<td>0.85</td>
<td>10</td>
<td>0.4</td>
<td>0.85</td>
<td>15</td>
<td>-1.3</td>
</tr>
<tr>
<td>1.35</td>
<td>10</td>
<td>0.04</td>
<td>0.79</td>
<td>18</td>
<td>-1.9</td>
</tr>
<tr>
<td>1.35</td>
<td>10</td>
<td>0.4</td>
<td>0.85</td>
<td>20</td>
<td>-1.9</td>
</tr>
<tr>
<td>0.35</td>
<td>50</td>
<td>0.04</td>
<td>0.79</td>
<td>46</td>
<td>-3.8</td>
</tr>
<tr>
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<td>50</td>
<td>0.4</td>
<td>0.85</td>
<td>51</td>
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</tr>
<tr>
<td>0.85</td>
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<td>0.79</td>
<td>71</td>
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</tr>
<tr>
<td>0.85</td>
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<td>0.4</td>
<td>0.85</td>
<td>80</td>
<td>-8.5</td>
</tr>
<tr>
<td>1.35</td>
<td>50</td>
<td>0.04</td>
<td>0.79</td>
<td>97</td>
<td>-12</td>
</tr>
<tr>
<td>1.35</td>
<td>50</td>
<td>0.4</td>
<td>0.85</td>
<td>110</td>
<td>-12</td>
</tr>
</tbody>
</table>
seen that the current density has little influence on $Tr$. The difference is caused by the small change in $V_{be}$. Furthermore table 2 shows that emitter length has little and emitter width has much influence on $Tr$.

<table>
<thead>
<tr>
<th>emitter-length ($\mu m$)</th>
<th>emitter-width ($\mu m$)</th>
<th>$Tr$ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$J=0.04$ mA/$\mu m^2$</td>
</tr>
<tr>
<td>10</td>
<td>0.35</td>
<td>9.8</td>
</tr>
<tr>
<td>20</td>
<td>0.35</td>
<td>9.2</td>
</tr>
<tr>
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<tr>
<td>10</td>
<td>0.85</td>
<td>4.7</td>
</tr>
<tr>
<td>20</td>
<td>0.85</td>
<td>4.7</td>
</tr>
<tr>
<td>50</td>
<td>0.85</td>
<td>4.6</td>
</tr>
<tr>
<td>10</td>
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<td>3.9</td>
</tr>
<tr>
<td>20</td>
<td>1.35</td>
<td>3.9</td>
</tr>
<tr>
<td>50</td>
<td>1.35</td>
<td>3.9</td>
</tr>
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</table>
APPENDIX C APPLICATION OF THE CHARGE-CONTROL MODEL FOR TRANSIENT ANALYSIS OF ECL CIRCUITS

1 INTRODUCTION

In the frequency divider, being a digital circuit, the transistors act as a switch that can be 'on' or 'off'. During the switching from 'on' ('off') to 'off' ('on') large voltage and current variations may occur. For the calculation of the turn-on (turn-off) time, the time required for a transistor to switch from the off (on)-condition to the on (off)-condition, we need a transistor model that describes the dynamic or transient properties of the transistor.

For this application the small signal model is inaccurate because of the large voltage and current variations that are involved in digital circuits. The MEXTRAM model is too complex and not very suited for transient hand analysis. The Charge-control model [12] offers a solution.

In this appendix we will discuss the application of the Charge-control model for transient analysis of ECL circuits. We will first discuss the Charge-control transistor model and we will present the model equations. Then the transient characteristics of the current switch, the basic building block of ECL circuits are discussed. We will calculate the switching times using the Charge-control model and compare the calculations with the results of computer simulations. In this way information is obtained about the validity and accuracy of the Charge-control analysis.

2 THE CHARGE-CONTROL MODEL

In the Charge-control model the transistor is no longer described as a current controlled device, that is \( I_C = h_{fe} I_B \) \((I_C\text{ and } I_B\text{ are the collector and base current, } h_{fe}\text{ is the DC current gain})\), but as a charge controlled device. In this charge controlled device the well known relation:

\[ Q_B = I_C T_r \]  

(1)
is used. Here $Q_b$ is the minority carrier charge in the neutral base and $T_f$ the forward transit time. The base current is described as:

$$I_b = \frac{Q_b}{h r e T_f} + \frac{dQ_b}{dt}$$  \hspace{1cm} (2)

The first term in (2) represents the loss of minority carriers in the base region because of recombination with the majority carriers, and the majority carrier current injected by the base into the emitter. The second term is introduced to account for the time rate of change of $Q_b$ in the neutral base region of the transistor. The first part of the equation is the steady-state term; the second part is the transient term.

The emitter current is the sum of the base and collector current. In figure 1 this simple Charge-control model of the transistor is shown.

![fig. 1 The simple Charge-control model for the npn transistor](image-url)
So far attention has been focused on the charge storage in the neutral base region of the transistor. But there is also charge stored in the depletion regions of the transistor. When we include the depletion capacitances and also the series resistances, according to the simplified MEXTRAM transistor model, the complete Charge-control equations become:

\[
I_b' = \frac{Q_b}{h_reTr} + \frac{dQ_b}{dt} + \frac{dQ_{te}}{dt} + \frac{dQ_{tc}}{dt}
\]

\[
I_c' = \frac{Q_b}{h_reTr} - \frac{dQ_{tc}}{dt} - \frac{dQ_{ts}}{dt}
\]

\[I_e' = I_c' + I_b'
\]

The complete Charge-control transistor model is shown in figure 2. The external emitter current, base current and collector current are denoted as \(I_e', I_b'\) and \(I_c'\) respectively.

For analytical calculations (3) is not very practical. We rather have a set of equations with only electrical circuit variables (voltage, current). Therefore we will rewrite (3). Integrating equations (3) and using relation (1) yields:

\[
\int_{t_0}^{t_1} I_b' dt = \int_{t_0}^{t_1} \frac{I_c}{h_re} dt + Tr\Delta I_c + \Delta Q_{te} + \Delta Q_{tc}
\]

\[
\int_{t_0}^{t_1} I_c' dt = \int_{t_0}^{t_1} I_c dt - \Delta Q_{tc} - \Delta Q_{ts}
\]

\[I_e' = I_c' + I_b'
\]

The \(\Delta\) denotes the change (in current or charge) between \(t= t_0\) and \(t= t_1\).
fig. 2 The complete Charge-control model for the npn transistor

The depletion charge $\Delta Q_t$ can be calculated with:

$$\Delta Q_t = Q_t(t_1) - Q_t(t_0) = \int_{V_0}^{V_1} C_t(V) dV,$$

(5)

where $V_0$ and $V_1$ are the junction voltages at $t = t_0$ and $t = t_1$. $C_t(V)$ is the voltage dependant and non-linear depletion capacitance:

$$C_t(V) = C_t(1 - \frac{V}{V_d})^{-p},$$

(6)
with $C_t$ the zero bias depletion capacitance, $V$ the junction voltage, $V_d$ the built-in junction voltage and $p$ the grading coefficient.

Substitution of (6) in (5) and using $\Delta V = V_1 - V_0$ yields:

$$\Delta Q_t = C_{eq} \Delta V,$$  \hspace{1cm} (7)

with $C_{eq}$ the large signal equivalent depletion capacitance:

$$C_{eq} = \frac{-V_d}{\Delta V(1-p)} \left[ (1- \frac{V_1}{V_d})^{1-p} - (1- \frac{V_0}{V_d})^{1-p} \right] C_t.$$  \hspace{1cm} (8)

Equations (4), (7) and (8) form the Charge-control equations which will be used in the Charge-control analysis.

In ECL circuits transistors operate in two modes, the cut-off mode and the forward active mode. In cut-off mode the base-emitter voltage $V_{be}$ is so small that a negligible collector current flows. In forward active mode the transistor conducts the 'on-current' $I_q$. For the Charge-control model this implies that in cut-off mode we can neglect $Q_b = I_c T_r$. The transition between the cut-off and the forward active mode is determined by the turn-on base-emitter voltage $V_{be}(on)$. We will define $V_{be}(on)$ as the base-emitter voltage where $I_c$ is one percent of $I_q$. So when $I_c < I_q/100$ or $V_{be} < V_{be}(on)$ the transistor is assumed to be in cut-off mode. From the ideal diode equation $V_{be} = V_T \ln(I_c/I_o)$, with $V_T$ the thermal voltage ($V_T = 26 \text{ mV at } T = 300 \text{ K}$) and $I_o$ the saturation current, we can write for $V_{be}(on)$:

$$V_{be}(on) = V_{be}(I_c=I_q/100) = V_{be}(I_c=I_q) - V_T \ln(100) = V_{be}(I_c=I_q) - 120 \text{ mV}.$$  

The turn-on base-emitter voltage depends on the electrical transistor parameters and the 'on-current density'. For the BASIC transistor $V_{be}(on) = 0.67 \text{ Volt}$ for a 'on-current density' of 40 $\mu A/\mu m^2$ and $V_{be}(on) = 0.73 \text{ Volt}$ for a 'on-current density' of 400 $\mu A/\mu m^2$. 

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For the current switch, shown in figure 3.a, we will calculate the turn-on and the turn-off time and verify the calculations with the results of simulations. In figure 3.b the equivalent charge control model is shown. For simplicity all resistors except $R_{be}$ are equal to zero.

For this circuit it can be verified that, using the ideal transistor equation, the ratio between $I_{e1}'$ and $I_{e2}'$ is equal to:

$$
\frac{I_{e1}'}{I_{e2}'} = e^{\frac{(V_{11}-V_{12})}{V_T}}
$$

with $V_T$ the thermal voltage ($V_T = 26$ mV for $T=300$ K). So with the differential input voltage $V_{in} = V_{11} - V_{12}$ sufficient positive $I_{e1}' \approx I_{gate}$ and $I_{e2}' \approx 0$.

When $V_{in}$ changes from negative to positive, $T_1$ turns on and $I_{e1}'$ becomes $I_{gate}$. Also when $V_{in}$ changes from positive to negative, $T_1$ turns off and $I_{e1}'$ becomes zero.

Assume $V_{11}$ is a rectangular pulse which at time $t_1$ abruptly changes from $-2-V_{i/2}$ to $-2+V_{i/2}$ and $V_{12}$ is a rectangular pulse which at time $t_1$ abruptly changes from $-2+V_{i/2}$ to $-2-V_{i/2}$. Here $V_i$ is the differential voltage swing. The DC voltage of the inputs is chosen as $-2$ Volt.

The turn-on sequence is shown in figure 4. In figure 3.b the corresponding voltages and currents are denoted. The input voltage $V_{11}$, the collector current $I_{e1}'$, the internal base voltage $V_B$ and the internal collector current $I_{e1}$ are shown. The turn-on sequence can be described as follows:

With $V_{11}$ at $-2-V_{i/2}$ transistor $T_1$ is cut off, so $I_{e1}=I_{e1}'=0$. Following the step input at time $t_1$ there is no change in $I_{e1}$, until $t_2$. This delay time is due to the voltage across the emitter and collector junctions being unable to change instantaneously due to the depletion capacitances. After $t_2$ $V_{b\text{e}1} > V_{b\text{e}(on)}$ so the transistor is in forward active mode and starts conducting current.
Numerical values:

- $V_{ee} = -5$ Volt
- $V_I = 0.5$ Volt
- $V_e = -2.85$ Volt
- $P_e = 0.37$
- $P_c = 0.19$
- $V_{de} = 0.98$
- $V_{dc} = 0.60$

**fig. 3** (a) Circuit diagram of current switch; (b) Charge-Control equivalent current switch model.
From $t_2$ to $t_3$ there is a rise time of $I_{c1}$. This time delay is again due to the depletion capacitances, but now also includes the supply of the neutral base charge $Q_b$. Finally after $t_3$ the external collector current $I_{c1}'$ takes over $I_{c1}$ and becomes at $t_4$ equal to $I_{gate}/2$. The delay between $I_{c1}$ and $I_{c1}'$ is caused by the base-collector capacitance.

At some time $t_5$ there is another step change in the input voltage. $V_{il}$ changes from $-2+V_l/2$ to $-2-V_l/2$ and $V_{l2}$ changes from $-2-V_l/2$ to $-2+V_l/2$. After $t_5$ both the base charge and the depletion charge of transistor $T_1$ is removed causing $I_{c1}$ to decrease immediately at $t_5$ and, after a short delay, also $I_{c1}'$ starts to decrease at $t_6$. At $t_7$ $I_{c1}'$ is equal to $I_{gate}/2$.

**fig. 4** Voltage and current waveforms of the current switch.
We see that, in contrast with the turn-on sequence, the transistor is only forward active during the turn-off sequence.

With the definition of the turn-on (turn-off) time as the time between the step change in input voltage and \( I_{c1} \) equal to \( I_{gate}/2 \), we have:

\[
\begin{align*}
\text{turn-on time} & \quad t_{on} = t_4 - t_1 \\
\text{turn-off time} & \quad t_{off} = t_7 - t_5
\end{align*}
\]

We will now calculate \( t_{on} \) and \( t_{off} \) using the Charge-control model shown in figure 3.b.

For the calculation of \( t_{on} \) and \( t_{off} \) we assume that the voltages and currents behave as shown in figure 4. We also assume that the common emitter voltage \( V_e \) does not change.

We first calculate \( t_{on} \). This calculation is separated into three parts. First the delay \( t_2 - t_1 \) then the delay \( t_3 - t_2 \) and finally the delay \( t_4 - t_3 \) is calculated.

The calculation of the delay \( t_2 - t_1 \) is done as follows:

At \( t_1 \) the transistor is cut off. Between \( t_1 \) and \( t_2 \) depletion charge is supplied by the base current. For the change in junction voltages we have, with \( V_{bel}=V_b-V_e \) (see figure 3.b),

\[
\Delta V_{be1} = V_{be1}(t_2) - V_{be1}(t_1) = (-2-V_e) - (-2-V_1/2-V_e) = V_1/2.
\]

With the collector voltage unchanged at 0 Volt it follows that

\[
\Delta Q_{ts1} = Q_{ts1}(t_2) - Q_{ts1}(t_1) = 0 .
\]

For the change of the base collector voltage we have, with \( V_{bc1}=V_b \)

\[
\Delta V_{bc1} = V_{bc1}(t_2) - V_{bc1}(t_1) = (-2) - (-2-V_1/2) = V_1/2.
\]
This change in junction voltage implies a change in charge. The change in charge is caused by the current $I_{b1}'$ which flows through $R_{bc}$ under the influence of $V_{11}$. The initial base current, at $t_1$, is (see fig. 4)

$$I_{b1}'(t_1) = \frac{V_{11}(t_1)-V_b(t_1)}{R_{bc}} = \frac{V_1}{R_{bc}}$$

but, at $t_2$,

$$I_{b1}'(t_2) = \frac{V_{11}(t_2)-V_b(t_2)}{R_{bc}} = \frac{V_1/2}{R_{bc}}.$$

Therefore the average current is given simply as

$$\overline{I_{b1}'} = \frac{V_1+V_1/2}{2R_{bc}} = \frac{3V_1}{4R_{bc}}. \quad (9)$$

Using (4.a) and (7) we then have

$$\int_{t_1}^{t_2} I_{b1}'(t) dt = \overline{I_{b1}'}(t_2-t_1) = C_{eqe}\Delta V_{bei} + C_{eqc}\Delta V_{bec}, \quad (10)$$

with $C_{eqe}$, $C_{eqc}$ the large signal depletion capacitance, according to (8), of respectively $C_{te}$ and $C_{tc}$. Calculating $C_{eqe}$ and $C_{eqc}$ with (8), using the numerical values shown in figure 4 we obtain

$$C_{eqe} = 1.37 \ C_{te} \quad (11)$$

$$C_{eqc} = 0.71 \ C_{tc}. \quad (11)$$

Substitution of (9) and (11) in (10) yields for $t_2-t_1$

$$\begin{align*}
\frac{t_2-t_1}{\overline{I_{b1}'}} &= \frac{C_{eqe}\Delta V_{bei} + C_{eqc}\Delta V_{bec}}{3V_1/(4R_{bc})} \\
&= \frac{1.37C_{te}V_1/2 + 0.71C_{tc}V_1/2}{3V_1/(4R_{bc})} \\
&= 0.91R_{bc}C_{te} + 0.47R_{bc}C_{tc}. \quad (12)
\end{align*}$$

The calculation of the delay $t_3-t_2$ is done as follows:

After $t_2$ the transistor is in forward active mode. This means that $V_{bei(on)} >= V_{bei(on)}$ and therefore the collector current starts flowing resulting in $I_{c1} = I_{gate}/2$ at time $t_3$.

$I_{c1}$ is related to the base charge $Q_{b1}$ as $I_{c1} = Q_{b1}/T_{ri}$. Therefore
between $t_2$ and $t_3$ this charge must be supplied by the base current. The base charge is given as

$$Q_b(t_2) = I_{c1}(t_2)T_f = 0$$

$$Q_b(t_3) = I_{c1}(t_3)T_f = I_{gate}T_f/2$$

hence,

$$\Delta Q_b = Q_b(t_3) - Q_b(t_2) = I_{gate}T_f/2.$$ 

During the interval $(t_2, t_3)$ the base voltage is almost constant and its value is approximately $-2$ Volt (see fig. 4). Hence there is no change in junction voltages and therefore no depletion charge is supplied between time $t_2$ and time $t_3$.

For the average base current we have

$$\overline{I_{b1'}} = \frac{V_{I1}-V_b}{R_{bc}} = \frac{-2+V_1/2- -2}{R_{bc}} = \frac{V_1}{2R_{bc}}.$$ 

For the collector current we assume a linear increase between $t_2$ and $t_3$ so

$$I_{c1}(t) = \frac{I_{gate}(t-t_2)}{2(t_3-t_2)}, \quad t_2 < t < t_3.$$ 

We now have for the Charge-control equation (4.a)

$$\int_{t_2}^{t_3} I_{b1'}(t) dt = \int_{t_2}^{t_3} \overline{I_{b1'}}(t_3-t_2) = \frac{V_1}{2R_{bc}}(t_3-t_2)$$

$$= \int_{t_2}^{t_3} \frac{I_{gate}(t-t_2)}{2h_f}(t_3-t_2) dt + I_{gate}T_f/2.$$ 

Rewriting the equation yields

$$t_3-t_2 = \frac{I_{gate}T_f/2}{V_1 - \frac{I_{gate}}{4h_f}}.$$ 

With $I_{gate}/(4h_f) \ll V_1/2R_{bc}$ we can simplify the formula

$$t_3-t_2 = \frac{I_{gate}T_fR_{bc}/V_1}{2R_{bc}I_{gate}T_f}$$

(13)
The calculation of the delay $t_4 - t_3$ is done as follows:

After $t_3$, $I_{c1}'$ starts flowing. With equation (4.b) we can calculate the delay $t_4 - t_3$. For $I_{c1}'$ we assume a linear increase between $t_3$ and $t_4$, so

$$I_{c1}'(t) = \frac{I_{gat}e(t-t_3)}{2(t_4-t_3)} , \quad t_3 < t < t_4 .$$

We also assume an average value for $I_{c1}$ between $t_3$ and $t_4$

$$\overline{I_{c1}}(t) = I_{gat}e , \quad t_3 < t < t_4 .$$

For the change in base-collector voltage we have with figure 4

$$\Delta V_{bc} = \Delta V_{be} = V_{be1}(t_4) - V_{be1}(t_3) \approx V_1/2$$

The large signal base-collector capacitance can be calculated as

$$C_{eqc} = 0.76C_{tc} .$$

We then have with (4.a)

$$\int_{t_3}^{t_4} \frac{I_{gat}e(t-t_3)}{2(t_4-t_3)} dt = \int_{t_3}^{t_4} I_{gat}e dt - 0.76C_{tc}V_1/2 .$$

Hence we can write, with $V_1 = 0.5$ V,

$$t_4 - t_3 = 0.25 \frac{C_{tc}}{I_{gat}e} \quad (14)$$

Delays (12), (13) and (14) together form the turn-on time

$$t_{on} = R_{bc}(0.91C_{tc}+0.47C_{tc}+2I_{gat}eTr)+0.25C_{tc}/I_{gat}e \quad (15)$$

The calculation of the turn-off time can be done using the results of the previous calculations. During the turn-off time $t_7-t_5$ the change in depletion charge and base charge is the same as in the time interval $(t_2,t_4)$. Only now the base current flows in opposite
direction. Therefore \( t_7 - t_5 = t_4 - t_2 \) so

\[
t_{\text{off}} = 2*R_{bc} I_{\text{gate}} T_r + 0.25 C_{tc}/I_{\text{gate}} \quad (16)
\]

We see that \( t_{\text{on}} \) and \( t_{\text{off}} \) are weighted sums of time constants. The weighting factors are determined by the circuit, the electrical parameters and the input voltage swing.

It is informative to compare the hand calculations of the switching times with computer simulations. For the current switch of figure 3 the simulated voltage and current wave forms are shown in figure 5. It can be seen that the collector current approximately behaves as we have assumed.

In table 1 the calculated and simulated switching times are listed for two different current densities and for zero and non-zero \( R_{bv} \). Considering first the case of \( R_{bv} = 0 \) we see in table 1 that the calculated \( t_{\text{on}} \) is fairly accurate but the calculated \( t_{\text{off}} \) is somewhat too high for \( I_{\text{gate}} = 0.68 \text{ mA} \). The discrepancies are caused by the assumptions we made in order to simplify the hand calculations. The accuracy of the hand calculations determines the accuracy of the weighting factors. A better and more accurate Charge-control analysis is possible, but we will not carry out this analysis because this will only result in somewhat more accurate weighting factors at the expense of much more hand calculations.

In table 1 it can be seen that when \( R_{bv} \) is 67 \( \Omega \) in stead of zero the increase of delay is small although the total base resistance \((R_{bc}+R_{bv})\) almost doubles. The reason for this is the strong current crowding that occurs during the turn-on and turn-off sequence. The current crowding is caused by the large base currents that are flowing during switching. We therefore can neglect the influence of \( R_{bv} \) without loosing too much accuracy, provided that \( R_{bv} \) is not much larger than \( R_{bc} \). This simplifies the Charge-control model considerably.

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Fig. 5 Simulation of the transient response of the current switch \(w=0.85\), \(l=18.85\), \(I_{\text{gate}}=6.8\) mA).

<table>
<thead>
<tr>
<th>(I_{\text{gate}}) (mA)</th>
<th>(R_{\text{Bv}}) (Ω)</th>
<th>calculated (t_{\text{on}}) (ps)</th>
<th>calculated (t_{\text{off}}) (ps)</th>
<th>simulated (t_{\text{on}}) (ps)</th>
<th>simulated (t_{\text{off}}) (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.68</td>
<td>0</td>
<td>21.5</td>
<td>14.9</td>
<td>20</td>
<td>9.3</td>
</tr>
<tr>
<td>6.8</td>
<td>0</td>
<td>13.9</td>
<td>7.4</td>
<td>14.2</td>
<td>7.5</td>
</tr>
<tr>
<td>0.68</td>
<td>67</td>
<td>21.5</td>
<td>14.9</td>
<td>22</td>
<td>10.3</td>
</tr>
<tr>
<td>6.8</td>
<td>67</td>
<td>13.9</td>
<td>7.4</td>
<td>16.7</td>
<td>7.8</td>
</tr>
</tbody>
</table>

Table 1 Switching times of current switch. \(w=0.85\) μm, \(l=18.85\) μm \(R_{\text{bc}}=84\) Ω, \(R_{\text{cc}}=R_{\text{cv}}=R_{\text{e}}=0\), \(C_{\text{tc}}=39\) fF, \(C_{\text{te}}=64\) fF, \(T_r=4.9\) ps.